

TSMC65: LVDS Pad Set



Libraries

| Name | Process | CUP | Form Factor |
|-----------------------------|---------|-----|-------------|
| RGO_TSMC65_25V25_LP_UC_LVDS | LP | yes | staggered |

Summary

The LVDS I/O is a three-module design (input, output and reference block). The LDP_OU_675_25V_T is a 1350MBit/s LVDS Driver, LDP_IN_675_25V_DN is a 900MBit/s LVDS Receiver and the LDP_RE_000_25V is the voltage reference for up to 16 drivers. The LDP_OU_675_25V_T is designed to drive either 50Ω or 100Ω differential termination. This cell has been designed to meet a set of the standard LVDS specifications (IEEE Std 1596.3-1996, Low Voltage Differential Signaling).

These pads will generally be used at frequencies of less than 400 MHz. Using this LVDS Pad Set, the system can achieve very high data rates per pin with simple termination requirements and low EMI. Both driver and receiver have been optimized for speed/power and can be ported to various pure digital CMOS processes from 0.18μm down to 45nm technologies. The LDP_OU_675_25V_T has been optimized for 1350MBit/s operations. The receiver has been designed with no hysteresis in order to optimize sensitivity and skew.

The driver design has all the necessary components for transmit of LVDS data and a temperature stable internal reference for setting of the LVDS signaling voltage and common mode level. This provides user flexibility in deploying multiple LVDS transmitters. The reference block is required for the LVDS drivers to provide a stable common mode voltage as well as an accurate current reference for the driver source / sink current. Maximum operating frequency is 675 MHz.

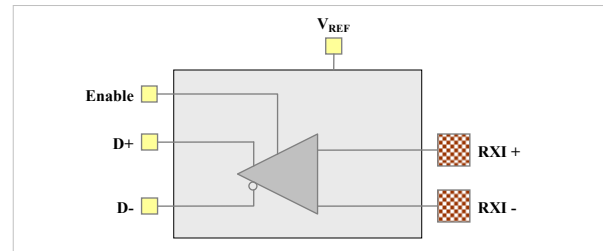
Absolute maximum ratings

| Symbol | Description | Value | Units |
|-------------------|--------------------------------------|-----------------------------------|-------|
| V _{VDD} | Core supply voltage range | -0.5 to 1.38 | V |
| V _{DVDD} | I/O supply voltage range | -0.5 to 2.95 | V |
| V _{PAD} | Voltage range at PAD | -0.5 to (V _{DVDD} + 0.5) | V |
| T _J | Junction operating temperature range | -55 to 150 | °C |

Recommended operating conditions

| Symbol | Description | Min | Nom | Max | Units |
|-------------------|-------------------------------|-------|------------|-------------------------|-------|
| V _{VDD} | Core supply voltage | 0.9 | 1.0 to 1.2 | 1.32 | V |
| V _{DVDD} | I/O supply voltage | 2.25 | 2.5 | 2.75 | V |
| V _{VREF} | Reference voltage | | | | V |
| T _A | Ambient operating temperature | 0 | 25 | 100 | °C |
| T _J | Junction temperature | -40 | 25 | 125 | °C |
| V _{PAD} | Voltage at PAD | -0.3V | | V _{DVDD} +0.3V | V |

LDP_IN_675_25V_DN: 450MHz LVDS Input



Key features:

- Powered from 2.5V ±10% and 1.0V to 1.2V (±10%) core power supplies
- Operates up to 450 MHz (900Mbps)
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Common mode range from 0V to 2.4V (limited by Power Supply)
- Power-up sequence independent
- Power consumption is 7 mW typical and 10 mW maximum

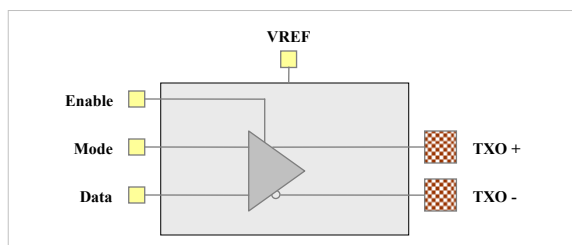
AC Characteristics

| Parameter | Typ | Max | Units | Conditions |
|-----------------------------|-----|-----|-------|---|
| Propagation delay | 1.7 | 2.0 | ns | The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns |
| Maximum operating frequency | 450 | | MHz | All noise, jitter, and t _{dcd} measured at 450 MHz |
| Maximum data rate | 900 | | Mb/s | |

TSMC65: LVDS Pad Set



LDP_OU_675_25V_T: 675 MHz LVDS Output Pad



Key features:

- Powered from 2.5V $\pm 10\%$ and 1.0V to 1.2V ($\pm 10\%$) core power supplies
- Operates up to 675 MHz (1350Mbps)

AC Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|------------|--|--|-----|------|-----|-------|
| t_{PHL} | Differential high to low propagation delay | $R_L = 100 \Omega$ $C_L = 1 \text{ pF}$ | 700 | 1200 | | ps |
| t_{PLH} | Differential low to high propagation delay | $R_L = 100 \Omega$ $C_L = 1 \text{ pF}$ | 700 | 1200 | | ps |
| t_{rise} | V_{OD} differential rise time | 20% to 80% | 150 | 300 | | ps |
| t_{fall} | V_{OD} differential fall time | 20% to 80% | 150 | 300 | | ps |

Characterization Corners

| Nominal VDD | Model | VDD | DVDD = 2.5V | Temperature |
|-------------|-------|---------|-------------|-------------|
| 1.2 | FF | +10% | +10% | -40°C |
| | FF | +10% | +10% | 125°C |
| | TT | nominal | nominal | 25°C |
| | SS | -10% | -10% | -40°C |
| 1.0 | SS | -10% | -10% | 125°C |
| | FF | +10% | +10% | -40°C |
| | FF | +10% | +10% | 125°C |
| | TT | nominal | nominal | 25°C |
| | SS | -10% | -10% | -40°C |
| | SS | -10% | -10% | 125°C |

Cell summary

| Name | Description |
|-------------------|--|
| LDP_IN_675_25V_DN | 450 MHz LVDS input cell |
| LDP_OU_675_25V_T | 675 MHz LVDS output cell |
| LDP_RE_000_25V | VREF pad |
| PVP_VD_RCD_12V | Core power pad with VREF |
| PVP_VS_RCD_12V | Power pad for VSS with VREF bus |
| PVP_VD_PDO_25V | Driver power pad with POC control |
| PVP_VD_RDO_25V | Driver power pad |
| PVP_VS_RDO_25V | I/O ground supply with VREF bus |
| SVP_SP_001_25V | 0.1 μm spacer |
| SVP_SP_001_25V | 1 μm spacer |
| SVP_SP_005_25V | 5 μm spacer |
| SVP_SP_010_25V | 10 μm spacer |
| SPP_RS_005_25V | DVDD, DVSS, POC, BIAS and VREF rail splitter |
| SPP_SPC_AD_UN | Core limited library adapter pad |

Physical sizes

| Pad name | Width | Height[*] | Units |
|-------------------|-------|-----------|---------------|
| LDP_RE_000_18V | 70 | 190 | μm |
| LDP_IN_675_25V_DN | 60 | 190 | μm |
| LDP_OU_675_25V_T | 65 | 190 | μm |
| PVP_VD_RCD_12V | 30 | 180 | μm |
| PVP_VS_RCD_12V | 30 | 180 | μm |
| PVP_VD_PDO_25V | 30 | 180 | μm |
| PVP_VD_RDO_25V | 30 | 180 | μm |
| PVP_VS_RDO_25V | 30 | 180 | μm |
| SVP_SP_000_25V | 0.1 | 180 | μm |
| SVP_SP_001_25V | 1 | 180 | μm |
| SVP_SP_005_25V | 5 | 180 | μm |
| SVP_SP_010_25V | 10 | 180 | μm |
| SPP_RS_005_25V | 5 | 180 | μm |
| SPP_SPC_AD_UN | 25 | 180 | μm |

[*] Includes CUP bond opening.

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