TSMC40: (R)GMII



Libraries

Name	Process	Form Factor
RGO TSMC40 25V33 LP 30C RGMII	LP	Staggered CUP

Summary

The (R)GMII library provides the combo driver / receiver cell for both Gigabit Media Independent Interface signaling and Reduced Gigabit Media Independent Interface signaling. It is designed to interface Ethernet PHY to network switch ASICs. This library is provided as a supplement to the 40nm GPIO libraries provided by Aragio Solutions.

GMII Specification Compliant:

IEEE 802.3-2005

RGMII Specification Compliant

HP RGMII, version 1.3, 12/10/2000

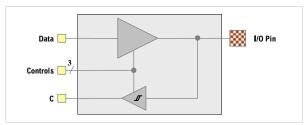
ESD Protection:

- JEDEC compliant
 - o 2KV ESD Human Body Model (HBM)
 - o 200 V ESD Machine Model (MM)
 - o 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of ± 100mA @ 125°C

MIP_BI_SDS_33V_SCB



(R)GMII Combo Driver Features:

- Selectable output slew rate
- GMII mode powered by 3.3V I/O & 1,1V core supplies
- RGMII mode powered by 2.5V I/O & 1.1V core supplies

Pad Size

Pad	Width	Height	Units
MIP BI SDS 33V SCB	30	180	μm

Recommended operating conditions

V _{VDD} Core supply voltage 0.99 1.1 1.21 V T _J Junction temperature -40 25 +125 °C V _{PAD} Voltage at IO 0 V _{DVDD} V V _{DVDD} I/O supply voltage 2.97 3.3 3.63 V V _{IH} Input logic high 1.7 - - V V _{IL} Input logic low 1.9 - - V V _{OH} Output logic low voltage 0 - 0.7 V V _{DVDD} I/O supply voltage 2.25 2.5 2.75 V V _{IH} Input logic low 1.7 - - 0.5 V V _{DVDD} I/O supply voltage 2.25 2.5 2.75 V V _{IH} Input logic low 1.7 - - 0.7 V V _{IH} Input logic low 1.7 - - 0.7 V V _{IH} Input logic high voltage 1.7		Description		Min	No m	Max	Units
V _{PAD} Voltage at IO 0 V _{DVDD} V V _{DVDD} I/O supply voltage 2.97 3.3 3.63 V V _{IH} Input logic high 1.7 - - V V _{IL} Ac Input logic low voltage, AC - 0.9 V V _{OH} Ac Input low voltage, AC - 0.7 V V _{OH} Output logic low voltage 0 - 0.5 V V _{IH} Input logic low voltage 2.25 2.5 2.75 V V _{IH} Input logic low 1.7 - - V V _{IH} Input logic low 1.7 - - V V _{IH} Input logic low 1.7 - - V V _{OH} Output logic low voltage - 0.7 V V _{OH} Output logic low voltage - 0.7 V V _{OL} Output logic low voltage - 0.3 0.4 V V _{OL} Output logic low voltage - 0.3 0.4 V	V_{VDD}	Core supply voltage		0.99	1.1	1.21	V
V _{DVDD} VO supply voltage V _{IL} Input logic high V _{IL} Input logic low V _{IL} Input logic low voltage, AC V _{OH} Output logic high voltage V _{OL} Output logic low voltage V _{IL} Input logic high voltage V _{IL} Input logic low V _{IL} Input logic low V _{IL} Input logic low V _{OH} Output logic high voltage V _{OL} Output logic high voltage V _{OL} Output logic low voltage V _{OL}	T_{J}	Junction temperature		-40	25	+125	°C
Note	V_{PAD}	Voltage at IO		0		V_{DVDD}	V
V _{IL} Ac Input logic low Input logic low<	V_{DVDD}	I/O supply voltage		2.97	3.3	3.63	V
V _{IL_AC} Input high voltage, AC V V _{IH_AC} Input low voltage, AC - - 0.7 V V _{OH} Output logic high voltage 2.1 - 3.6 V V _{DVDD} I/O supply voltage 0 - 0.5 V V _{IH} Input logic high 1.7 - - V V _{IL} Input logic low - 0.7 V V _{OH} Output logic high voltage 2.0 - V _{DVDD} +0.3 V _{OL} Output logic low voltage V _{Dvvss} - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + MH-2	V_{IH}	Input logic high		1.7	-	-	V
V _{IH_AC} Input low voltage, AC - - 0.7 V V _{OH} Output logic high voltage 2.1 - 3.6 V V _{DVDD} I/O supply voltage 0 - 0.5 V V _{IH} Input logic high 2.25 2.5 2.75 V V _{IL} Input logic low 1.7 - - V V _{OH} Output logic high voltage 2.0 - V _{DVDD} V +0.3 V _{DVSS} - 0.3 - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + MIL-	V_{IL}	Input logic low	_	-	-	0.9	V
V _{IH_AC} Input low voltage, AC - - 0.7 V V _{OH} Output logic high voltage 2.1 - 3.6 V V _{DVDD} I/O supply voltage 0 - 0.5 V V _{IH} Input logic high 2.25 2.5 2.75 V V _{IL} Input logic low 1.7 - - V V _{OH} Output logic high voltage 2.0 - V _{DVDD} V +0.3 V _{DVSS} - 0.3 - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + MIL-	V_{IL_AC}	Input high voltage, AC	M	1.9	-	-	V
Vol. Output logic low voltage 0 - 0.5 V V _{DVDD} I/O supply voltage 2.25 2.5 2.75 V V _{IH} Input logic high 1.7 - - V V _{OL} Output logic low 5 2.0 - V _{DVDD} V +0.3 V _{OL} Output logic low voltage V _{DVSS} - 0.3 - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + MLI-	$V_{\text{IH_AC}}$	Input low voltage, AC		-	-	0.7	V
V _{DVDD} I/O supply voltage	V_{OH}	Output logic high voltage		2.1	-	3.6	V
V _{IH} Input logic high 1.7 - - V V _{IL} Input logic low - - 0.7 V V _{OH} Output logic high voltage 2.0 - V _{DVDD} +0.3 V V _{OL} Output logic low voltage V _{DVSS} - 0.3 - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + MI-	V_{OL}	Output logic low voltage		0	-	0.5	V
V _{IL} Input logic low So - - 0.7 V V _{OH} Output logic high voltage 2.0 - V _{DVDD} +0.3 V V _{OL} Output logic low voltage V _{DVSS} - 0.3 - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + NAI-	V_{DVDD}	I/O supply voltage		2.25	2.5	2.75	V
V _{OH} Output logic high voltage	V_{IH}	Input logic high		1.7	-	-	V
V _{OL} Output logic low voltage V _{DVSS} - 0.4 V F Clock frequency / 2.5 ^[1] - 125 + MI	V_{IL}	Input logic low	₹	-	-	0.7	V
F Clock frequency / 2.5 ^[1] - 125 + MI	V_{OH}	Output logic high voltage	RG	2.0	-		V
	V _{OL}	Output logic low voltage		0.3	-	0.4	V
accuracy 100ppm 100ppm	F	Clock frequency / accuracy		2.5 ^[1] - 100ppm		125 + 100ppm	MHz

^[1] The lowest supported frequency is 10BASE-T over RGMII

Power Dissipation

Mode	Min	Nom	Max	Units
GMII	48	60	74	μW/MHz
RGMII	31	39	50	μW/MHz

RMS Current - GMII

Parameter	Min	Nom	Max	Unit
I _{DVDD ms}	2.4	3.3	4.5	mA
I _{VDD rms}	0.11	0.14	0.26	mA

RMS Current – RGMII

Parameter	Min	Nom	Max	Unit
I _{DVDD ms}	2.2	3.1	4.5	mA
IVDD rms	0.12	0.13	0.27	mA

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Characterization Corners

Nominal VDD	Model	VDD	DVDD ^[1]	Temperature
	FF	+10%	+10%	-40°C
	FF	+10%	+10%	0°C
	FF	+10%	+10%	125°C
1.1	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	125°C

^[1] DVDD = 2.5 and 3.3V

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