## **TSMC40:** ONFI 3.0



## Libraries

| Name                         | Process | Form Factor   |
|------------------------------|---------|---------------|
| RGO_TSMC40_25V33_LP_30C_ONFI | LP      | Staggered CUP |
| RGO TSMC40 25V33 LP 50C ONFI | LP      | Inline CUP    |

## **Summary**

The ONFI library provides the combo driver / receiver cells, the ODT / driver impedance calibration cell, and the voltage reference cell to support both single-ended and differential ONFI 3.0 signaling. This library also meets the requirements for Toggle 2.0 signaling. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated ONFI domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- ONFI 3.0 Single-Ended Driver /Receiver
- ONFI 3.0 Differential Clock Driver / Receiver
- ODT / Z<sub>O</sub> Calibration Cell
- Voltage Reference

The ONFI I/O library supports all impedance modes defined in the ONFI 3.0 specification and features fast and precise calibration, low power consumption, area-efficient design, and easy integration into the physical layer (PHY).

#### **ESD Protection:**

- JEDEC compliant
  - o 2KV ESD Human Body Model (HBM)
  - o 200 V ESD Machine Model (MM)
  - o 500 V ESD Charge Device Model (CDM)

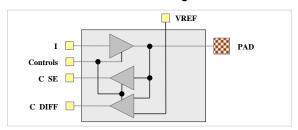
## Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

## **Recommended operating conditions**

| Symbo                | I Description                  | Min                     | Nom | Max                     | Units |
|----------------------|--------------------------------|-------------------------|-----|-------------------------|-------|
| $V_{VDD}$            | Core supply voltage            | 0.99                    | 1.1 | 1.21                    | V     |
| $V_{DVDD}$           | I/O augustu valtaga            | 1.62                    | 1.8 | 1.98                    | V     |
|                      | I/O supply voltage             | 2.7                     | 3.3 | 3.6                     | V     |
| TJ                   | Junction temperature           | -40                     | 25  | 125                     | °C    |
| $V_{PAD}$            | Voltage at PAD                 | -0.3V                   |     | V <sub>DVDD</sub> +0.3V | ′ V   |
| V <sub>IH (DC)</sub> | Input High (DC)                | 0.7 * V <sub>DVDD</sub> |     | $V_{DVDD} + 0.3$        | V     |
| V <sub>IL (DC)</sub> | Input Low (DC)                 | V <sub>DVSS</sub> - 0.3 |     | 0.3 * V <sub>DVDD</sub> | V     |
| V <sub>IH (AC)</sub> | Input High (AC)                | 0.8 * V <sub>DVDD</sub> |     | $V_{DVDD} + 0.3$        | V     |
| V <sub>IL (AC)</sub> | Input Low (AC)                 | V <sub>DVSS</sub> - 0.3 |     | 0.2 * V <sub>DVDD</sub> | V     |
| V <sub>IH (DC)</sub> | Input High (DC)                | V <sub>REF</sub> +.125  |     | $V_{DVDD} + 0.3$        | V     |
| V <sub>IL (DC)</sub> | Input Low (DC)                 | V <sub>DVSS</sub> - 0.3 |     | V <sub>REF</sub> 125    | V     |
| V <sub>IH (AC)</sub> | Input Low (DC) Input High (AC) | V <sub>REF</sub> +.250  |     |                         | V     |
| V <sub>IL (AC)</sub> | Input Low (AC)                 |                         |     | V <sub>REF</sub> 125    | V     |

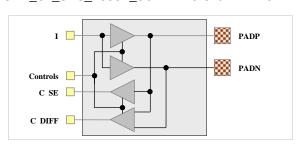
## ONP\_BI\_SDS\_1833V\_SCB: Single-Ended Driver



#### ONFI Single-Ended Driver / Receiver Features:

- Driver user-selectable on-die termination and programmable drive strength with ODT / Z<sub>0</sub> calibration and programmable "off" state control.
  - ODT  $R_{tt} = 30\Omega / 50\Omega / 75\Omega / 100\Omega / 150\Omega$
  - $Z_{OUT} = \frac{18\Omega}{25\Omega} / \frac{35\Omega}{35\Omega} / \frac{50\Omega}{35\Omega}$
  - Off state Z / pull-up / pull-down / bus keeper
- Receiver single-ended and pseudo-differential outputs
- Powered by 1.8V / 3.3V I/O and 1.1V core supplies
- Maximum operating frequency 200 MHz

## ONP\_CL\_SDS\_1833V\_SCB: Differential Driver



#### **ONFI Differential Clock Driver / Receiver Features:**

- Driver user-selectable on-die termination and programmable drive strength with ODT / Z<sub>O</sub> calibration and programmable "off" state control.
  - $\circ ODT R_{tt} = 30\Omega / 50\Omega / 75\Omega / 100\Omega / 150\Omega$
  - $Z_{OUT} = 18\Omega / 25\Omega / 35\Omega / 50\Omega$
  - Off state Z / pull-up / pull-down / bus keeper
- Receiver single-ended and true differential outputs
- Powered by 1.8V / 3.3V I/O and 1.1V / 1.2V core supplies
- Maximum operating frequency 200 MHz

## **Characterization Corners**

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| <b>Nominal VDD</b> | Model | VDD     | DVDD [1] | Temperature |
|--------------------|-------|---------|----------|-------------|
| 1.1V               | FF    | +10%    | +10%     | -40°C       |
|                    | FF    | +10%    | +10%     | 125°C       |
|                    | TT    | nominal | nominal  | 25°C        |
|                    | SS    | -10%    | -10%     | -40°C       |
|                    | SS    | -10%    | -10%     | 125°C       |

[1] DVDD voltages - 1.8V, 3.0V and 3.3V.

# **TSMC40: ONFI 3.0**



## **Cell summary**

| Name                 | Description  |
|----------------------|--|
|                      |  |
|                      | ONFI 3.0 Single-Ended Driver/Receiver  |
| ONP_CL_SDS_1833V_SCB | ONFI 3.0 Differential Clock Driver/Receiver  |
| ONP_SP_CAL_1833V     | Calibration cell   |
| ONP_RE_000_1833V     | Voltage Reference (VREF).  |
| ANP_BI_DWR_33V       | Analog IO cell with two inputs to core: 1. $600\Omega$ series R for ESD, 2. Less than $10\Omega$ |
| PVP_VD_PDO_1833V     | I/O V <sub>DD</sub> (DVDD) with POC  |
| PVP_VD_RDO_1833V     | I/O V <sub>DD</sub> (DVDD)   |
| PVP_VS_RDO_1833V     | I/O V <sub>SS</sub> (DVSS)   |
| PVP_VS_DRC_1833V     | I/O V <sub>SS</sub> (DVSS is shorted to VSS)   |
| PVP_VD_RCD_11V       | Core V <sub>DD</sub> (VDD)   |
| PVP_VS_RCD_11V       | Core V <sub>SS</sub> (VSS)   |
| PVP_VS_DRC_11V       | Core V <sub>SS</sub> (DVSS is shorted to VSS)  |
| SVP_CO_001_1833V     | Corner cell  |
| SVP_SP_000_1833V     | 0.1µm spacer cell  |
| SVP_SP_001_1833V     | 1µm spacer cell  |
| SVP_SP_005_1833V     | 5µm spacer cell  |
| SVP_SP_020_1833V     | 20µm spacer cell   |
| SPP_RS_005_1833V     | Rail splitter cell (breaks DVDD, DVSS, VREF, CAL_DWHVx[30], POC and HVPS)                        |
| SPP_SP_CAP_1833V     | Core decap cell  |

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