TSMC40: LVDS

Libraries

Name	Process	Form Factor
RGO_TSMC40_25V25_LP_UC_LVDS	LP	Staggered CUP

Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 2.0 Gbps. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- 1.2 GHz LVDS Driver
- 1.0 GHz LVDS Receiver
- LVDS Voltage Reference

LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 200 V ESD Machine Model (MM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

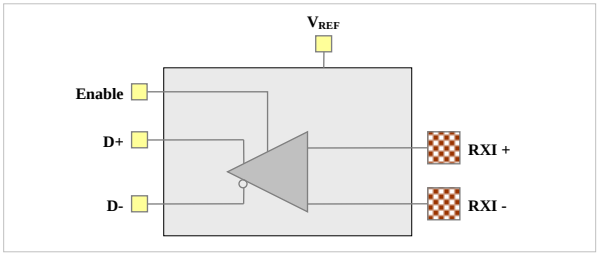
Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.99	1.1	1.21	V
V_{DVDD}	I/O supply voltage	2.25	2.5	2.75	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 2.5V	Temperature
1.1	FF	+10%	+10%	-40°C
	FF	+10%	+10%	0°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	125°C

LDP_IN_675_25V_DN: 1.0GHz LVDS Input



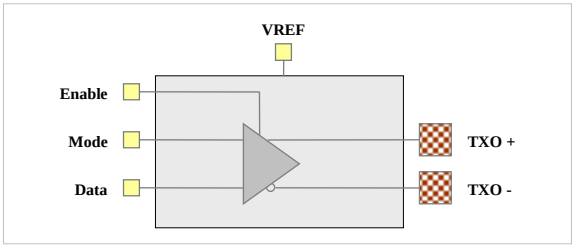
LVDS Receiver Features:

- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Common mode range from 0V to 2.5V (limited by power supply)
- Powered by 2.5V I/O and 1.1V core supplies
- Power consumption: 9.75 mW max @ 1GHz

AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation delay	0.9	1.23	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns
Maximum operating frequency	1.0		GHz	All noise, jitter, and tdcd measured at 1GHz
Maximum data rate	2.0		Gb/s	

LDP_OU_675_25V_T: 1.2GHz LVDS Output



LVDS Driver Features:

- Operates up to 1.2GHz (2.4Gbps) with external 1 pF load
- Common mode output range 1.2V ±100mV
- Differential Skew between TXO_P and TXO_N 20ps
- High and low current drive modes to support 50Ω and 100Ω differential terminations
- Powered by 2.5V I/O and 1.1V core supplies
- Power consumption: 26.8 mW max

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t_{PHL}	Differential high to low propagation delay	R_L = 100 Ω C_L = 1 pF		530	630	ps
t_{PLH}	Differential low to high propagation delay	R_L = 100 Ω C_L = 1 pF		530	630	ps
t_{rise}	V_{OD} differential rise time	20% to 80%	190	230	250	ps
t_{fall}	V_{OD} differential fall time	20% to 80%	125	140	150	ps

Cell summary

Name	Description
LDP_IN_675_25V_DN	1GHz LVDS input cell
LDP_OU_675_25V_T	1GHz LVDS output cell
LDP_RE_000_25V	LVDS Voltage Reference cell
PVP_VD_RCD_11V	Core power (VDD)
PVP_VD_RC2_11V	Core power (VDD) – double width
PVP_VD_RC3_11V	Core power (VDD) – triple width
PVP_VS_RCD_11V	Core ground (VSS)
PVP_VS_RC2_11V	Core ground (VSS) – double width
PVP_VS_RC3_11V	Core ground (VSS) – triple width
PVP_VD_PDO_25V	I/O power (DVDD) with POC control
PVP_VD_RDO_25V	I/O power (DVDD)
PVP_VS_RDO_25V	I/O ground (VSS)
SVP_SP_000_25V	0.1 µm spacer
SVP_SP_001_25V	1 µm spacer
SVP_SP_005_25V	5 µm spacer
SVP_SP_010_25V	10 µm spacer
SPP_RS_005_25V	DVDD, DVSS, POC, BIAS & VREF rail splitter

Physical sizes

Pad name	Width	Height[*]	Units
LDP_RE_000_25V	60	190	µm
LDP_IN_675_25V_DN	60	190	µm
LDP_OU_675_25V_T	70	190	µm
PVP_VD_RCD_12V	30	180	µm
PVP_VD_RC2_11V	60	180	µm
PVP_VD_RC3_11V	90	180	µm
PVP_VS_RCD_12V	30	180	µm
PVP_VS_RC2_11V	60	180	µm
PVP_VS_RC3_11V	90	180	µm
PVP_VD_PDO_25V	30	180	µm
PVP_VD_RDO_25V	30	180	µm
PVP_VS_RDO_25V	30	180	µm
SVP_SP_000_25V	0.1	180	µm
SVP_SP_001_25V	1	180	µm
SVP_SP_005_25V	5	180	µm
SVP_SP_010_25V	10	180	µm
SPP_RS_005_25V	5	180	µm

[*] Includes CUP bond opening.

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