# SMIC40: subLVDS



## Libraries

Name		Process	Form Factor	
RGO SMIC40	25V18 LL U	SUBLVDS	LL	Staggered CUP

## **Summary**

The subLVDS library provides a subLVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 1600 Mbps. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated subLVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- 800 MHz LVDS Driver
- 800 MHz LVDS Receiver
- subLVDS Voltage Reference

## subLVDS Specification Compliant:

SMIA 1.0 PART 2: CCP2 Specification

#### **ESD Protection:**

- JEDEC compliant
  - o 2KV ESD Human Body Model (HBM)
  - o 200 V ESD Machine Model (MM)
  - o 500 V ESD Charge Device Model (CDM)

#### Latch-up Immunity:

- JEDEC compliant
  - o Tested to I-Test criteria of ± 100mA @ 125°C

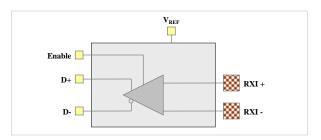
## **Recommended operating conditions**

Symbo	ol Description	Min	Nom	Max	Units
$V_{VDD}$	Core supply voltage	0.99	1.1	1.21	V
$V_{DVDD}$	I/O supply voltage	1.62	1.8	1.98	V
TJ	Junction temperature	-40	25	125	°C
$V_{PAD}$	Voltage at PAD	-0.3V		V <sub>DVDD</sub> +0.3	VV

# **Characterization Corners**

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
1.1	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

# LDP IN 675 18V DN: 800 MHz subLVDS Input



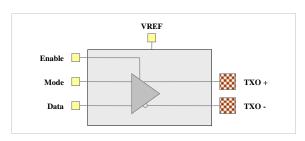
#### subLVDS Receiver Features:

- Input receive sensitivity of 50mV peak differential (without hysteresis)
- Common mode range from 0.4V to 1.6V (limited by Power Supply)
- Powered by 1.8V I/O and 1.1V core supplies
- Power consumption: 3.4 mW max @ 800 MHz

#### **AC Characteristics**

Parameter	Тур	Max	Units	Conditions
Propagation delay	0.80	1.1	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns
Maximum operating frequency	800		MHz	All noise, jitter, and tdcd measured at 800 MHz
Maximum data rate	1600		Mb/s	

# LDP\_OU\_675\_18V\_T: 800 MHz subLVDS Output



#### subLVDS Driver Features:

- Operates up to 800 MHz (1600 Mbps) with 1 pF load
- Common mode output range 900mV ±100mV
- Differential Skew between TXO\_P and TXO\_N 20ps
- High and low current drive modes to support  $50\Omega$  and  $100\Omega$  differential terminations
- Powered by 1.8V I/O and 1.1V core supplies
- Power consumption: 18.1 mW typ & 25.2 mW max

# **AC Characteristics**

Symb	ol Description	Condition	Min	Тур	Max	Units
t <sub>PHL</sub>	Differential high to low propagation delay	$R_L = 100 \Omega$ $C_L = 1 pF$		600	820	ps
t <sub>PLH</sub>	Differential low to high propagation delay	$R_L = 100 \Omega$ $C_L = 1 pF$		600	820	ps
t <sub>rise</sub>	V <sub>OD</sub> differential rise time	20% to 80%	120	140	190	ps
t <sub>fall</sub>	V <sub>OD</sub> differential fall time	20% to 80%	120	140	190	ps

# SMIC40: subLVDS



# **Cell summary**

Name	Description
LDP_IN_450_18V_DN	800 MHz subLVDS input cell
LDP_OU_450_18V_T	800 MHz subLVDS output cell
LDP_RE_000_18V	subLVDS Voltage Reference cell
PVP_VD_RCD_12V	Core power (VDD)
PVP_VS_RCD_12V	Core ground (VSS)
PVP_VD_PDO_18V	I/O power (DVDD) with POC control
PVP_VD_RDO_18V	I/O power (DVDD)
PVP_VS_RDO_18V	I/O ground (VSS)
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 μm spacer
SVP_SP_005_18V	5 μm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPP_AD_UN	Inline to staggered adapter

# **Physical sizes**

Pad name	Width	Height <sup>[*]</sup>	Units
LDP_IN_450_18V_DN	27.5	180	μm
LDP_OU_450_18V_T	55	180	μm
LDP_RE_000_18V	55	180	μm
PVP_VD_RCD_12V	20	180	μm
PVP_VS_RCD_12V	20	180	μm
PVP_VD_PDO_18V	20	180	μm
PVP_VD_RDO_18V	20	180	μm
PVP_VS_RDO_18V	20	180	μm
SVP_SP_000_18V	0.1	180	μm
SVP_SP_001_18V	1	180	μm
SVP_SP_005_18V	5	180	μm
SVP_SP_010_18V	10	180	μm
SPP_RS_005_18V	5	180	μm
SPC SPP AD UN	20	180	μm

[\*] Includes CUP bond opening.

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