SMIC40: subLVDS

Libraries

Name	Process	Form Factor
RGO_SMIC40_25V18_LL_UC_SUBLVDS	LL	Staggered CUP

Summary

The subLVDS library provides a subLVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 1600 Mbps. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated subLVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- 800 MHz LVDS Driver
- 800 MHz LVDS Receiver
- subLVDS Voltage Reference

subLVDS Specification Compliant:

- SMIA 1.0 PART 2: CCP2 Specification

ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 200 V ESD Machine Model (MM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

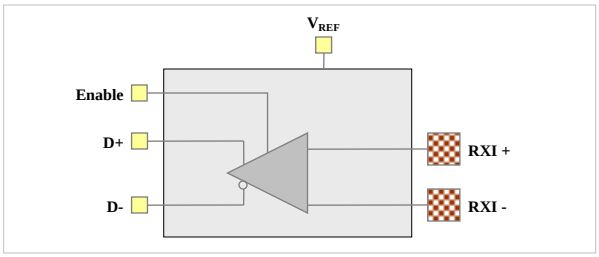
Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.99	1.1	1.21	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
1.1	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

LDP_IN_675_18V_DN: 800 MHz subLVDS Input



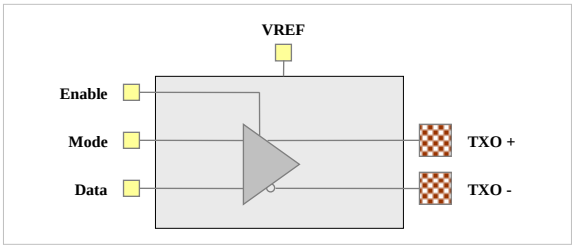
subLVDS Receiver Features:

- Input receive sensitivity of 50mV peak differential (without hysteresis)
- Common mode range from 0.4V to 1.6V (limited by Power Supply)
- Powered by 1.8V I/O and 1.1V core supplies
- Power consumption: 3.4 mW max @ 800 MHz

AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation delay	0.80	1.1	ns	The slew rate for propagation delays, duty cycle distortion and maximum operating frequency are 1V/ns
Maximum operating frequency	800		MHz	All noise, jitter, and tdcd measured at 800 MHz
Maximum data rate	1600		Mb/s	

LDP_OU_675_18V_T: 800 MHz subLVDS Output



subLVDS Driver Features:

- Operates up to 800 MHz (1600 Mbps) with 1 pF load
- Common mode output range 900mV ±100mV
- Differential Skew between TXO_P and TXO_N 20ps
- High and low current drive modes to support 50Ω and 100Ω differential terminations
- Powered by 1.8V I/O and 1.1V core supplies
- Power consumption: 18.1 mW typ & 25.2 mW max

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t_{PHL}	Differential high to low propagation delay	R_L = 100 Ω C_L = 1 pF		600	820	ps
t_{PLH}	Differential low to high propagation delay	R_L = 100 Ω C_L = 1 pF		600	820	ps
t_{rise}	V_{OD} differential rise time	20% to 80%	120	140	190	ps
t_{fall}	V_{OD} differential fall time	20% to 80%	120	140	190	ps

SMIC40: subLVDS

Cell summary

Name	Description
LDP_IN_450_18V_DN	800 MHz subLVDS input cell
LDP_OU_450_18V_T	800 MHz subLVDS output cell
LDP_RE_000_18V	subLVDS Voltage Reference cell
PVP_VD_RCD_12V	Core power (VDD)
PVP_VS_RCD_12V	Core ground (VSS)
PVP_VD_PDO_18V	I/O power (DVDD) with POC control
PVP_VD_RDO_18V	I/O power (DVDD)
PVP_VS_RDO_18V	I/O ground (VSS)
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPP_AD_UN	Inline to staggered adapter

Physical sizes

Pad name	Width	Height[*]	Units
LDP_IN_450_18V_DN	27.5	180	µm
LDP_OU_450_18V_T	55	180	µm
LDP_RE_000_18V	55	180	µm
PVP_VD_RCD_12V	20	180	µm
PVP_VS_RCD_12V	20	180	µm
PVP_VD_PDO_18V	20	180	µm
PVP_VD_RDO_18V	20	180	µm
PVP_VS_RDO_18V	20	180	µm
SVP_SP_000_18V	0.1	180	µm
SVP_SP_001_18V	1	180	µm
SVP_SP_005_18V	5	180	µm
SVP_SP_010_18V	10	180	µm
SPP_RS_005_18V	5	180	µm
SPC_SPP_AD_UN	20	180	µm

[*] Includes CUP bond opening.

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