SMIC40: SSTL_15

Libraries

Name	Process	Form Factor
RGO_SMIC40_25V15_LL_30C_SSTL_15	LL	Staggered CUP

Summary

The SSTL_15 pad set supports bidirectional single-ended and differential SSTL_15 signaling. The driver/receiver pairs, with embedded power cells, are supplied with a full complement of calibration, voltage reference, power, spacer, and adapter cells to assemble a pad ring by abutment. An included rail splitter allows isolated SSTL_15 domains (1.5V) to be placed in the same pad ring with 2.5V/3.3V GPIO domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

Features:

- Full DDR3 capability - 800MHz (1600 MT/s)
- Low Power driving standard DDR3 memories
- User programmable ODT Capability - dynamic 6-Bit PVT calibration to an external reference resistor

ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 200 V ESD Machine Model (MM)
  - 500 V ESD Charge Device Model (CDM)

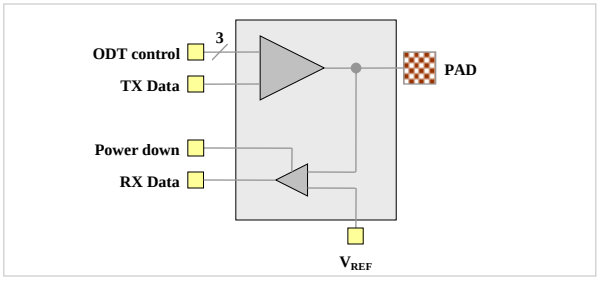
Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.99	1.1	1.21	V
V_{DVDD}	I/O supply voltage	1.425	1.5	1.575	V
V_{VREF}	Reference voltage	0.67	0.75	0.8	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	0		V_{DVDD}	V
$V_{IH\ (dc)}$	DC input logic high	V_{REF} + 0.1		V_{DVDD}	V
$V_{IL\ (dc)}$	DC input logic low	TBD		V_{REF} - 0.1	V
$V_{IH\ (ac)}$	AC input logic high	V_{REF} + 0.175		-	V
$V_{IL\ (ac)}$	AC input logic low	-		V_{REF} - 0.175	V

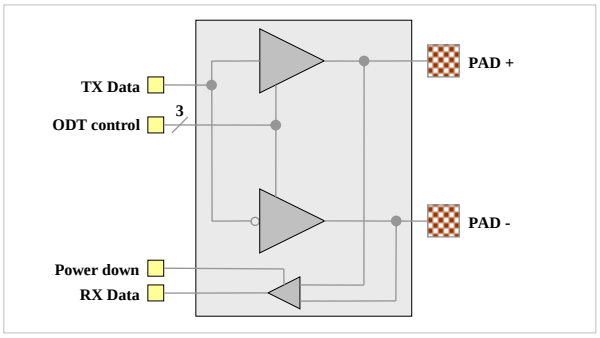
SLP_BI_SDS_15V_D – SSTL_15 Driver



AC Characteristics

Symbol	Parameter		Max	Unit
F	Max frequency		800	MHz
P_{DISS}	Power dissipation	800 MHz	10.2	mW

SLP_CL_SDS_15V_D – SSTL_15 Clock Driver



AC Characteristics

Symbol	Parameter		Max	Unit
F	Max frequency		800	MHz
P_{DISS}	Power dissipation	800 MHz	20.5	mW

SMIC40: SSTL_15

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.5V	Temperature
	FF	+10%	+5%	-40°C
	FF	+10%	+5%	125°C
1.1	TT	nominal	nominal	25°C
	SS	-10%	-5%	-40°C
	SS	-10%	-5%	125°C

Cell summary

Name	Description
SLP_BI_SDS_15V_D /DVDD/DVSS/PDO	SSTL_15 driver / receiver with power
SLP_CL_SDS_15V_D_PWR	Differential clock driver with DVDD/DVSS
SLP_SP_CAL_SDS_15V	SSTL_15 calibration pad
SLP_RE_000_15V	SSTL_15 voltage reference
PVP_VD_RCD_1215V	Core power (VDD)
PVP_VS_RCD_1215V	Core ground (VSS)
SVP_SP_000_15V	0.1 µm spacer
SVP_SP_001_15V	1 µm spacer
SVP_SP_005_15V	5 µm spacer
SVP_SP_010_15V	10 µm spacer
SPP_RS_005_15V	DVDD, DVSS, POC, CP[1..3], CN[1..3] and VREF rail splitter
SPP_AD_SSTL_15V	Adapter to staggered libraries
SVP_CO_001_15V	Corner cell

Physical sizes

Name	Width	Height	Units
SLP_BI_SDS_15V_D/DVDD/DVSS/PDO	55	170	µm
SLP_CL_SDS_15V_D_PWR	110	170	µm
SLP_SP_CAL_SDS_15V	55	170	µm
SLP_RE_000_15V	27.5	170	µm
PVP_VD_RCD_1215V	27.5	170	µm
PVP_VS_RCD_1215V	27.5	170	µm
SVP_SP_000_15V	0.1	170	µm
SVP_SP_001_15V	1	170	µm
SVP_SP_005_15V	5	170	µm
SVP_SP_010_15V	10	170	µm
SPP_RS_005_15V	5	170	µm
SPP_AD_SSTL_15V	25	180	µm
SVP_CO_001_15V	170	170	µm

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