

Libraries

Name	Process	Form Factor
RGO_SMIC40_25V15_LL_20C_SSTL_15_18	LL	Staggered CUP

Summary

The SSTL_15_18 combo pad set supports bidirectional single-ended and differential SSTL_15 and SSTL_18 signaling. The driver/receiver pairs, with embedded power cells, are supplied with a full complement of calibration, voltage reference, power, spacer, and adapter cells to assemble a pad ring by abutment. An included rail splitter allows isolated SSTLdomains (1.5V/1.8V) to be placed in the same pad ring with 2.5V/3.3V GPIO domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

Features:

- Full DDR3 capability - 800MHz (1600 MT/s)
- Full DDR2 capability
- Low Power driving standard DDR3 memories
- User programmable ODT Capability - dynamic 6-Bit PVT calibration to an external reference resistor

ESD Protection:

- JEDEC compliant
 - 2KV ESD Human Body Model (HBM)
 - 200 V ESD Machine Model (MM)
 - 500 V ESD Charge Device Model (CDM)

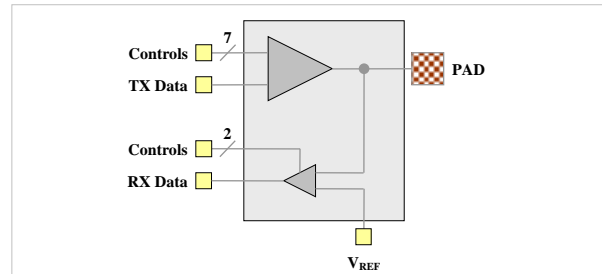
Latch-up Immunity:

- JEDEC compliant
 - Tested to I-Test criteria of $\pm 100\text{mA}$ @ 125°C

Recommended operating conditions

Description	Min	Nom	Max	Units
V _{VDD} Core supply	0.99	1.1	1.21	V
	1.08	1.2	1.26	V
V _{DVDD} I/O supply	SSTL_15 1.425	1.5	1.575	V
	SSTL_18 1.7	1.8	1.9	V
V _{VREF} Reference	.49 x V _{DVDD}	V _{DVDD}	.51 x V _{DVDD}	V
T _J Junction temp	-40	25	+125	°C
V _{PAD} PAD voltage	V _{DVSS}		V _{DVDD}	V
V _{IH} (DC) DC input logic high	SSTL_15 V _{REF} +100	-	V _{DVDD}	V
	SSTL_18 V _{REF} +125	-	V _{DVDD}	
V _{IL} (DC) DC input logic low	SSTL_15 V _{DVSS}	-	V _{REF} -100	V
	SSTL_18 V _{DVSS}	-	V _{REF} -125	
V _{IH} (AC) AC input logic high	SSTL_15 V _{REF} +175	-	-	V
	SSTL_18 V _{REF} +200	-	-	
V _{IL} (AC) AC input logic low	SSTL_15 -	-	V _{REF} -175	V
	SSTL_18 -	-	V _{REF} -200	

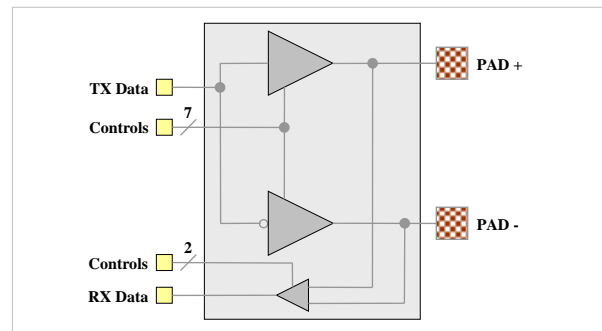
SLP_BI_SDS_18V_D – SSTL_15/18 Driver



AC Characteristics

Symbol	Parameter	Max	Unit
F	Max frequency	800	MHz
P _{DISS}	Power dissipation	SSTL_18 - 400 MHz	19.6 mW
		SSTL_15 - 800 MHz	10.2 mW

SLP_CL_SDS_18V_D – SSTL_15/18 Clock Driver



AC Characteristics

Symbol	Parameter	Max	Unit
F	Max frequency	800	MHz
P _{DISS}	Power dissipation	SSTL_18 - 400 MHz	61.3 mW
		SSTL_15 - 800 MHz	20.5 mW

Characterization Corners

Nominal VDD	Model	VDD	DVDD=1.5/1.8V	Temperature
1.1	FF	+10%	+5%	-40°C
	FF	+10%	+5%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-5%	-40°C
	SS	-10%	-5%	125°C

Cell summary

Name	Description
SLP_BI_SDS_18V_D	SSTL_15/18 Driver / receiver with power /DVDD/DVSS/PDO
SLP_CL_SDS_18V_D_PWR	Differential clock driver with DVDD/DVSS
SLP_SP_CAL_SDS_18V	SSTL_15 Calibration pad
SLP_RE_000_1518V	SSTL Voltage Reference
PVP_VD_RCD_1218V	Core power (VDD)
PVP_VS_RCD_1218V	Core ground (VSS)
SVP_SP_000_1518V	0.1 µm spacer
SVP_SP_001_1518V	1 µm spacer
SVP_SP_005_1518V	5 µm spacer
SVP_SP_010_1518V	10 µm spacer
SPP_RS_005_1518V	DVDD, DVSS, POC, CP[1..3], CN[1..3] and VREF rail splitter
SPP_AD_SSTL_1518V	Adapter to staggered libraries
SVP_CO_001_1518V	Corner cell

Physical size

Name	Width	Height	Units
SLP_BI_SDS_18V_D/DVDD/DVSS/PDO	55	240	µm
SLP_CL_SDS_18V_D_PWR	110	240	µm
SLP_SP_CAL_SDS_18V	27.5	240	µm
SLP_RE_000_1518V	27.5	240	µm
PVP_VD_RCD_1218V	27.5	240	µm
PVP_VS_RCD_1218V	27.5	240	µm
SVP_SP_000_1518V	0.1	240	µm
SVP_SP_001_1518V	1	240	µm
SVP_SP_005_1518V	5	240	µm
SVP_SP_010_1518V	10	240	µm
SPP_RS_005_1518V	5	240	µm
SPP_AD_SSTL_1518V	25	240	µm
SVP_CO_001_15V	240	240	µm

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Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: (972) 516-0999
Fax: (972) 516-0998
Web: <http://www.aragio.com/>

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