GF40: ONFI 3.0

Libraries

Name	Process	Form Factor
RGO_GF40_25V33_LP_30C_ONFI	LP	Staggered CUP

Summary

The ONFI library provides the combo driver / receiver cells, the ODT / driver impedance calibration cell, and the voltage reference cell to support both single-ended and differential ONFI 3.0 signaling. This library also meets the requirements for Toggle 2.0 signaling. The pad set includes a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated ONFI domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

- ONFI 3.0 Single-Ended Driver /Receiver
- ONFI 3.0 Differential Clock Driver / Receiver
- ODT / Z_O Calibration Cell
- Voltage Reference

The ONFI I/O library supports all impedance modes defined in the ONFI 3.0 specification and features fast and precise calibration, low power consumption, area-efficient design, and easy integration into the physical layer (PHY).

ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 200 V ESD Machine Model (MM)
  - 500 V ESD Charge Device Model (CDM)

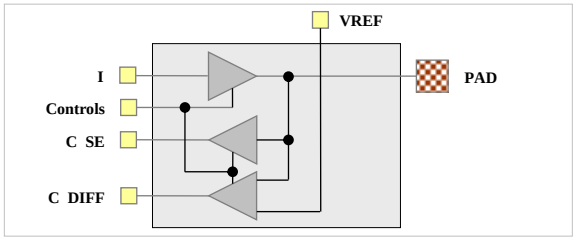
Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Recommended operating conditions

Symbol	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.99	1.1	1.21	V
			1.08	1.2	1.26	V
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
			2.7	3.3	3.6	
T_J	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at PAD		-0.3V		V_{DVDD}+0.3V	V
$V_{IH\ (DC)}$	Input High (DC)	NV-DDR	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
$V_{IL\ (DC)}$	Input Low (DC)	NV-DDR	V_{DVSS} - 0.3		0.3 * V_{DVDD}	V
$V_{IH\ (AC)}$	Input High (AC)	NV-DDR	0.8 * V_{DVDD}		V_{DVDD} + 0.3	V
$V_{IL\ (AC)}$	Input Low (AC)	NV-DDR	V_{DVSS} - 0.3		0.2 * V_{DVDD}	V
$V_{IH\ (DC)}$	Input High (DC)	NV-DDR2	V_{REF} +.125		V_{DVDD} + 0.3	V
$V_{IL\ (DC)}$	Input Low (DC)	NV-DDR2	V_{DVSS} - 0.3		V_{REF} -.125	V
$V_{IH\ (AC)}$	Input High (AC)	NV-DDR2	V_{REF} +.250			V
$V_{IL\ (AC)}$	Input Low (AC)	NV-DDR2			V_{REF} -.125	V

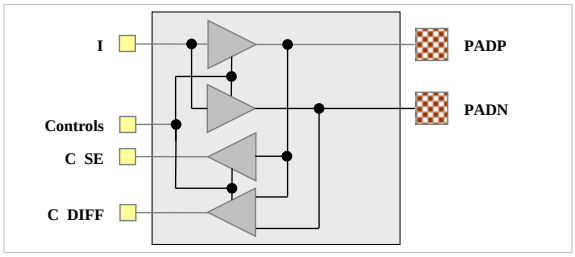
ONP_BI_SDS_1833V_SCB: Single-Ended Driver



ONFI Single-Ended Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_O calibration and programmable "off" state control.
  - ODT R_{tt} = 30Ω / 50Ω / 75Ω / 100Ω / 150Ω
  - Z_{OUT} = 18Ω / 25Ω / 35Ω / 50Ω
  - Off state – Z / pull-up / pull-down / bus keeper
- Receiver – single-ended and pseudo-differential outputs
- Powered by 1.8V / 3.3V I/O and 1.1V / 1.2V core supplies
- Maximum operating frequency – 200 MHz

ONP_CL_SDS_1833V_SCB: Differential Driver



ONFI Differential Clock Driver / Receiver Features:

- Driver – user-selectable on-die termination and programmable drive strength with ODT / Z_O calibration and programmable "off" state control.
  - ODT R_{tt} = 30Ω / 50Ω / 75Ω / 100Ω / 150Ω
  - Z_{OUT} = 18Ω / 25Ω / 35Ω / 50Ω
  - Off state – Z / pull-up / pull-down / bus keeper
- Receiver – single-ended and true differential outputs
- Powered by 1.8V / 3.3V I/O and 1.1V / 1.2V core supplies
- Maximum operating frequency – 200 MHz

Characterization Corners

Nominal VDD	Model	VDD	DVDD [1]	Temperature
1.2V	FF	+5%	+5%	-40°C
	FF	+5%	+5%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1V	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] DVDD voltages – 1.8V, 3.0V and 3.3V.

Cell summary

Name	Description
ONP_BI_SDS_1833V_SCB	ONFI 3.0 Single-Ended Driver/Receiver
ONP_CL_SDS_1833V_SCB	ONFI 3.0 Differential Clock Driver/Receiver
ONP_SP_CAL_1833V	Calibration cell
ONP_RE_000_1833V	Voltage Reference (VREF).
ANP_BI_DWR_33V	Analog IO cell with two inputs to core: 1. 600Ω series R for ESD, 2. Less than 10Ω
PVP_VD_PDO_1833V	I/O V_{DD} (DVDD) with POC
PVP_VD_RDO_1833V	I/O V_{DD} (DVDD)
PVP_VS_RDO_1833V	I/O V_{SS} (DVSS)
PVP_VS_DRC_1833V	I/O V_{SS} (DVSS is shorted to VSS)
PVP_VD_RCD_11V	Core V_{DD} (VDD)
PVP_VS_RCD_11V	Core V_{SS} (VSS)
PVP_VS_DRC_11V	Core V_{SS} (DVSS is shorted to VSS)
SVP_CO_001_1833V	Corner cell
SVP_SP_000_1833V	0.1µm spacer cell
SVP_SP_001_1833V	1µm spacer cell
SVP_SP_005_1833V	5µm spacer cell
SVP_SP_020_1833V	20µm spacer cell
SPP_RS_005_1833V	Rail splitter cell (breaks DVDD, DVSS, VREF, CAL_DWHVx[3..0], POC and HVPS)
SPP_SP_CAP_1833V	Core decap cell
SPP_AD_000_UN	Adapter cell

Physical sizes

Pad name	Width	Height[*]	Units
ONP_BI_SDS_1833V_SCB	30	360	µm
ONP_CL_SDS_1833V_SCB	60	360	µm
ONP_SP_CAL_1833V	30	360	µm
ONP_RE_000_1833V	30	360	µm
ANP_BI_DWR_33V	30	360	µm
PVP_VD_PDO_1833V	30	360	µm
PVP_VD_RDO_1833V	30	360	µm
PVP_VS_RDO_1833V	30	360	µm
PVP_VS_DRC_1833V	30	360	µm
PVP_VD_RCD_11V	30	360	µm
PVP_VS_RCD_11V	30	360	µm
PVP_VS_DRC_11V	30	360	µm
SVP_CO_001_1833V	360	360	µm
SVP_SP_000_1833V	0.1	360	µm
SVP_SP_001_1833V	1	360	µm
SVP_SP_005_1833V	5	360	µm
SVP_SP_020_1833V	20	360	µm
SPP_RS_005_1833V	5	360	µm
SPP_SP_CAP_1833V	10	10	µm
SPP_AD_000_UN	25	360	µm

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