

CSM65: MII Pad Set



Libraries

Name	Process	CUP	Form Factor
RGO_CSM65_25V33_G_30C_MII	G	yes	staggered
RGO_CSM65_25V33_LP_30C_MII	LP	yes	staggered
RGO_CSM65_25V33_G_50C_MII	G	yes	Inline
RGO_CSM65_25V33_LP_50C_MII	LP	yes	Inline

Summary

This library includes Mix_BI_004_5T_NC pad, designed to conform to the Reduced Media Independent Interface™ (RMII™) specification intended for use between Ethernet PHYs and Switch ASICs. Under IEEE 802.3u an MII comprised of 16 pins for data and control is defined. In devices incorporating many MACs or PHY interfaces such as switches, the number of pins can add significant cost as the port count increases. Typical switch products in the industry today offer 12 to 24 ports in a single device. At 6 pins per port and 1 pin per switch ASIC, the proposed RMII specification would save 119 pins plus the extra power and ground pins to support those additional pins for a 12 port switch ASIC.

The purpose of this interface is to provide a low cost alternative to the IEEE 802.3u MII. Architecturally, the RMII specification provides for an additional reconciliation layer on either side of the MII but can be implemented in the absence of an MII.

Power bus architecture and physical dimensions of this library are fully compatible with Aragio's standard I/O libraries

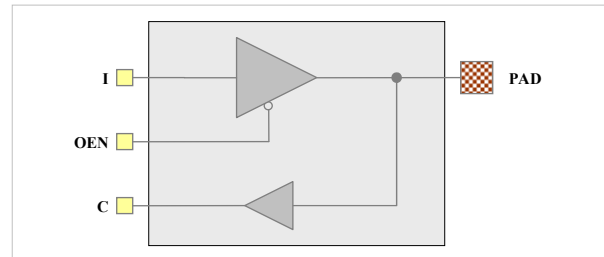
Features

- Capable of supporting 10 Mb/s and 100Mb/s data rates
- A single clock reference is sourced from MAC to PHY (or from an external source)
- It provides independent 2 bit wide (di-bit) transmit and receive data paths
- It uses TTL signal levels, compatible with common digital CMO ASIC processes
- Clock frequency of 50 MHz or less to minimize EMI and IC I/O requirements
- Pin count independent of port density of the PHY
- Single synchronous clocking
- Reduction of required control pins

Absolute maximum ratings

Symbol	Description	Value	Units
V _{VDD}	Core supply voltage range	-0.5 to 1.6	V
V _{DVDD}	I/O supply voltage range	-0.5 to 3.8	V
V _{PAD}	Voltage range at PAD	-0.5 to (V _{DVDD} + 0.5)	V
T _J	Junction operating temperature range	-55 to 150	°C

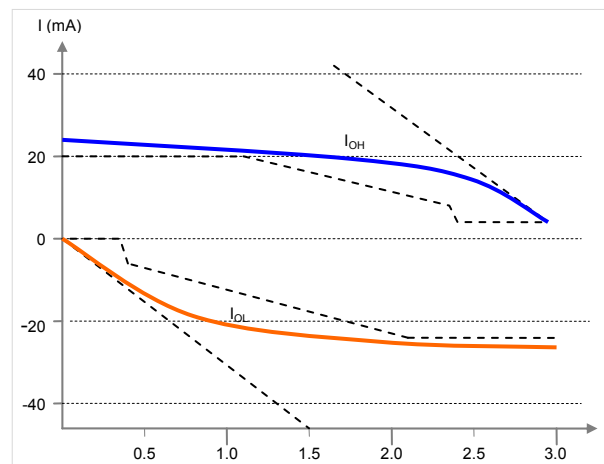
Mix_BI_004_33V_NC – MII I/O Pad



AC Characteristics

Symbol	Parameter	Max	Unit
F	Max frequency	25	MHz
P _{DISS}	Power dissipation	40.1	μW / MHz

Output Driver V-I Curve (Simulation Results)



Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V _{DVDD}	I/O supply voltage	2.97	3.30	3.63	V
T _A	Ambient operating temperature	0	25	100	°C
V _{VDD}	Core supply voltage	0.9	1.0 to 1.2	1.32	V
T _J	Junction temperature	-40	25	125	°C
V _{PAD}	Voltage at PAD	0		V _{DVDD}	V
V _{IH}	Input logic high	2.0		-	V
V _{IL}	Input logic low	-		0.8	V
V _{OH}	Output high	V _{DVDD} - 0.4		-	V
V _{OL}	Output low	-		0.4	V

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Characterization Corners

Nominal VDD	Model	VDD	DVDD = 3.3V	Temperature
1.2 ^[1]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1 ^[2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

^[1] LP process only.

^[2] G process only

Cell summary

Name	Description
MIP_BI_004_33V_NC	MII / RMII pad (staggered configuration)
MIC_BI_004_33V_NC	MII / RMII pad (inline configuration)

Physical size

Name	Width	Height	Units
MIP_BI_004_33V_NC	30	180	µm
MIC_BI_004_33V_NC	50	120	µm

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