CSM65: SSTL_2 Pad Set

Libraries

Name	Process	CUP	Form Factor
RGO_CSM65_25V25_G_30C_SSTL_2	G	yes	staggered
RGO_CSM65_25V25_LP_30C_SSTL_2	LP	yes	staggered

Summary

The SSTL_2 pad set is a full complement of I/O, power, and spacer cells (total of 14 cells) that are necessary to assemble a padring by abutment. Since the SSTL_2 normally operates with its own isolated power domain (2.5V), a "rail-splitter" support cell (SPP_RS_005_25V) is included to allow the designer to easily break the lines that should not connect to the rest of the padring, while allowing VDD and VSS to be continuous within the padring.
The cells are designed to provide the user with the option of either Class I or Class II operation that is fully compliant with the JEDEC standard JESD8-9B specification (250 MHz maximum frequency).
The reason for providing a pad set is because special control signals (POC, VREF) that are unique to the SSTL_2 I/O pads are routed through the padring. Therefore, the spacer and power supply pads must have these unique signals routed through. The VREF signal is placed to minimize any noise coupling. This enables the VREF pad (SLP_RE_000_25V) to support up to 40 SSTL_2 drivers or clock pads.

Features

- JEDEC standard compliant
- Supports both Class I and Class II

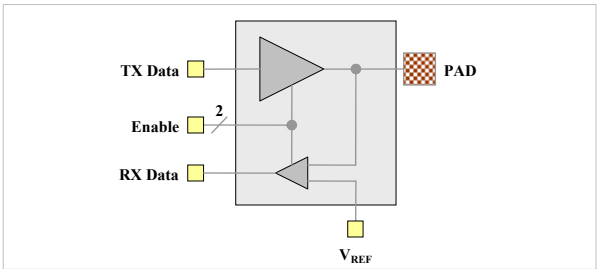
Absolute maximum ratings

Parameter	Description	Value	Units
V_{VDD}	Core supply voltage range	-0.5 to 1.4	V
V_{DVDD}	I/O supply voltage range	-0.5 to 2.75	V
V_{PAD}	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V
T_A	Storage temperature range	-55 to 150	°C

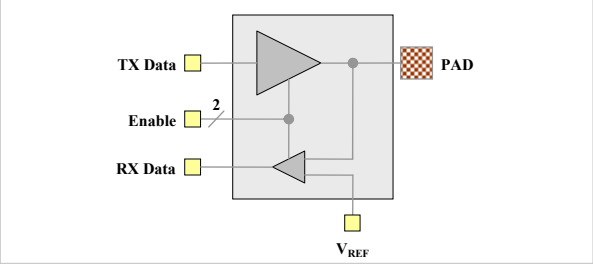
Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.90	1.0 to 1.2	1.32	V
V_{DVDD}	I/O supply voltage	2.25	2.5	2.75	V
V_{VREF}	Reference voltage	1.125	1.25	1.375	V
T_A	Ambient operating temperature	0	25	100	°C
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	0		V_{DVDD}	V
$V_{IH\ (dc)}$	DC input logic high	V_{REF}+125		V_{DVDD}+300	mV
$V_{IL\ (dc)}$	DC input logic low	-300		V_{REF}-125	mV
$V_{IH\ (ac)}$	AC input logic high	V_{REF}+250		-	mV
$V_{IL\ (ac)}$	AC input logic low	-		V_{REF}-250	mV

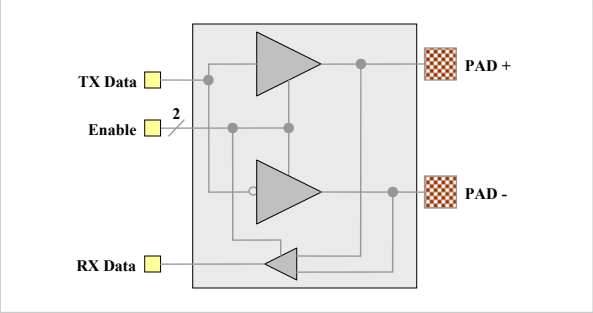
SLP_BI_008_25V_D – SSTL_2 Class I Driver



SLP_BI_016_25V_D – SSTL_2 Class II Driver



SLP_CL_008_25V_D – SSTL_2 Clock Driver



AC Characteristics

Symbol	Parameter	Max	Unit
F	Max frequency	250	V
P_{DISS}	Power dissipation	15	µW / MHz

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Characterization Corners

Nominal VDD	Model	VDD	DVDD = 2.5V	Temperature
1.2 [1]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1 [2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] LP process only.
[2] G process only.

Physical size

Name	Width	Height	Units
SLP_BI_008_25V_D	30	180	µm
SLP_BI_016_25V_D	30	180	µm
SLP_CL_008_25V_D	60	180	µm
SLP_RE_000_25V	30	180	µm
PVP_VD_RCD_12V	30	180	µm
PVP_VS_RCD_12V	30	180	µm
PVP_VD_PDO_25V	30	180	µm
PVP_VD_RDO_25V	30	180	µm
PVP_VS_RDO_25V	30	180	µm
SVP_SP_000_25V	0.1	180	µm
SVP_SP_001_25V	1	180	µm
SVP_SP_005_25V	5	180	µm
SVP_SP_010_25V	10	180	µm
SPP_RS_005_25V	5	180	µm
SPC_SPP_AD_UN	30	180	µm

Cell summary

Name	Description
SLP_BI_008_25V_D	SSTL_2 Class I driver
SLP_BI_016_25V_D	SSTL_2 Class II driver
SLP_CL_008_25V_D	SSTL_2 differential clock cell
SLP_RE_000_25V	SSTL_2 V_{REF} pad
PVP_VD_RCD_12V	Core V_{DD} with VREF bus
PVP_VS_RCD_12V	Core V_{SS} with VREF bus
PVP_VD_PDO_25V	I/O V_{DD} with POC control with VREF bus
PVP_VD_RDO_25V	I/O V_{DD} without POC with VREF bus
PVP_VS_RDO_25V	I/O V_{SS} with VREF bus
SVP_SP_000_25V	0.1 µm spacer
SVP_SP_001_25V	1 µm spacer
SVP_SP_005_25V	5 µm spacer
SVP_SP_010_25V	10 µm spacer
SPP_RS_005_25V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPP_AD_UN	Adapter cell to inline libraries

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