CSM65: subLVDS Pad Set

Libraries

Name	Process	CUP	Form Factor
RGO_CSM65_25V18_G_UC_SUBLVDS	G	yes	staggered
RGO_CSM65_25V18_LP_UC_SUBLVDS	LP	yes	staggered

Summary

The LVDS I/O is a three-module design (input, output and reference block). The LDP_OU_450_18V_T is a 900MBit/s LVDS Driver, LDP_IN_450_18V_DN is a 500MBit/s LVDS Receiver and the LDP_RE_000_18V is the voltage reference and current bias for up to 16 drivers. The LDP_OU_450_18V_T is designed to drive either 50Ω or 100Ω differential termination. This cell has been designed to meet the standard SubLVDS specifications (SMIA 1.0 Part 2:CCP2). Currently there is no standard for 50Ω termination

These pads will generally be used at frequencies of less than 400 MHz. Using this SubLVDS Pad Set, the system can achieve very high data rates per pin with simple termination requirements and low EMI. The driver has been optimized for speed/power and can be ported to various pure digital CMOS processes from 0.18µm down to 45nm technologies. The LDP_OU_450_18V_T has been optimized for 900MBit/s operations. The receiver has been designed with no hysteresis in order to optimize sensitivity and skew.

The driver design has all the necessary components for transmit of SubLVDS data and a temperature stable internal reference for setting of the SubLVDS signaling voltage and common mode level. This provides user flexibility in deploying multiple SubLVDS transmitters. The reference block is required for the SubLVDS drivers to provide a stable common mode voltage as well as an accurate current reference for the driver source / sink current. Maximum operating frequency is 450 MHz.

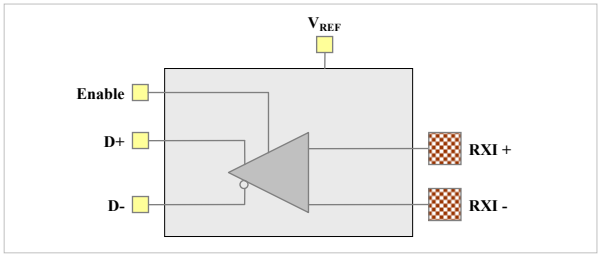
Absolute maximum ratings

Symbol	Description	Value	Units
V_{VDD}	Core supply voltage range	-0.5 to 1.38	V
V_{DVDD}	I/O supply voltage range	-0.5 to 2.95	V
V_{PAD}	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V
T_J	Junction operating temperature range	-55 to 150	°C

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.9	1.0 to 1.2	1.32	V
V_{DVDD}	I/O supply voltage	1.62	1.80	1.98	V
V_{VREF}	Reference voltage				V
T_A	Ambient operating temperature	0	25	100	°C
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V

LDP_IN_450_18V_DN: 250MHz SubLVDS Input



Key features:

- Powered from 1.8V ±10% and 1.0V to 1.2V (±10%) core power supplies
- Operates up to 250 MHz (500Mbps)
- Input receive sensitivity of 50mV peak differential (without hysteresis)
- Common mode range from 0.4V to 1.4V (limited by Power Supply)
- Power-up Sequence Independent
- Duty Cycle Distortion (DCD) less than 100ps
- Power consumption is 1.8 mW typical and 5 mW maximum

AC Characteristics

Parameter	Typ	Max	Units	Conditions
Propagation Delay	1.7	2.0	ns	
Input duty cycle distortion	50	100	ps	Minimum input swing, 100mV common mode noise from 50MHz to 1GHz
DVDD Power Supply Sensitivity	0.3	0.6	ps/mV	DVDD from -10% to -15% over all PVT, minimum input differential
VDD Power Supply Sensitivity	0.25	0.5	ps/mV	VDD from -10% to -15% over all PVT, minimum input differential
Maximum Operating Frequency	450		MHz	All noise, jitter, and tdcd measured at 450 MHz
Maximum Data Rate	900		Mb/s	
Power consumption	1.8	5.0	mW	

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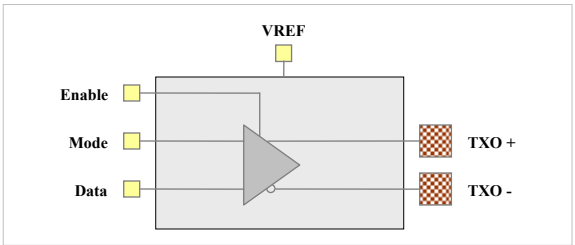
LDP_OU_450_18V_T: 450 MHz LVDS Output Pad



Key features:

- Powered from 1.8V ±10% and 1.0V to 1.2V (±10%) core power supplies
- Operates up to 450 MHz (900Mbps)

AC Characteristics

Symbol	Description	Condition	Min	Typ	Max	Units
t_{PHL}	Differential high to low propagation delay	R_L = 100 Ω C_L = 1 pF	550	750	1200	ps
t_{PLH}	Differential low to high propagation delay	R_L = 100 Ω C_L = 1 pF	550	750	1200	ps
t_{skew1}	Differential skew between t_{PHL} and t_{PLH}			100 [1]		ps
t_{skew2}	Channel-to-channel skew		-200	0	+200	ps
t_{rise}	V_{OD} differential rise time	20% to 80%	150		300	ps
t_{fall}	V_{OD} differential fall time	20% to 80%	150		300	ps

[1] The maximum differential skew (t_{skew1}) must be at least 100 pSec less than the actual Differential rise or fall times (t_{rise} or t_{fall}) at any specified valid operating condition.

Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
1.2 [1]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1 [2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] LP process only.
[2] G process only

Cell summary

Name	Description
LDP_IN_450_18V_DN	250 MHz SubLVDS input cell
LDP_OU_450_18V_T	450 MHz SubLVDS output cell
LDP_RE_000_18V	V_{REF} pad
PVP_VD_RCD_12V	Core power pad with VREF
PVP_VS_RCD_12V	Power pad for VSS with VREF bus
PVP_VD_PDO_18V	Driver power pad with POC control
PVP_VD_RDO_18V	Driver power pad
PVP_VS_RDO_18V	I/O ground supply with VREF bus
SVP_SP_001_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_SPC_AD_UN	Core limited library adapter pad

Physical sizes

Pad name	Width	Height[*]	Units
LDP_RE_000_18V	70	190	µm
LDP_IN_450_18V_DN	60	190	µm
LDP_OU_450_18V_T	65	190	µm
PVP_VD_RCD_12V	30	180	µm
PVP_VS_RCD_12V	30	180	µm
PVP_VD_PDO_18V	30	180	µm
PVP_VD_RDO_18V	30	180	µm
PVP_VS_RDO_18V	30	180	µm
SVP_SP_000_18V	0.1	180	µm
SVP_SP_001_18V	1	180	µm
SVP_SP_005_18V	5	180	µm
SVP_SP_010_18V	10	180	µm
SPP_RS_005_18V	5	180	µm
SPP_SPC_AD_UN	25	180	µm

[*] Includes CUP bond opening.

Published by:

Aragio Solutions
2201 K Avenue
Section B Suite 200
Plano, TX 75074-5918
Phone: **(972) 516-0999**
Fax: **(972) 516-0998**
Web: http://www.aragio.com/