CSM65: SSTL_18 Pad Set

Libraries

Name	Process	CUP	Form Factor
RGO_CSM65_25V18_G_30C_SSTL_18	G	yes	staggered
RGO_CSM65_25V18_LP_30C_SSTL_18	LP	yes	staggered

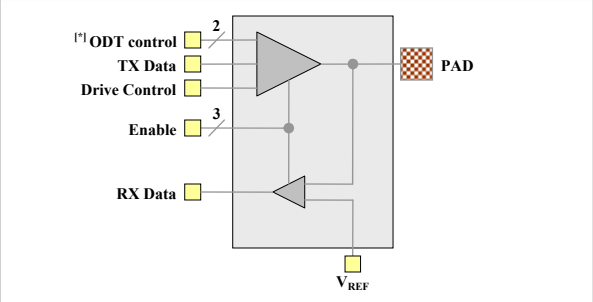
Summary

The SSTL_18 pad set is a full complement of I/O, power, and spacer cells that are necessary to assemble a padring by abutment. Since the SSTL_18 normally operates with its own isolated power domain (1.8V), a "rail-splitter" support cell (SPP_RS_005_18V) is included to allow the designer to easily break the lines that should not connect to the rest of the padring, while allowing VDD and VSS to be continuous within the padring. The output circuitry is designed with 2.5-volt FET's, but all parameters are guaranteed only at 1.8 volts (±10%).
The cells are designed to provide the user with the option of either 60% or full drive that is fully compliant with the JEDEC standard JESD8-15a specification up to 400 MHz (DDR800) with balanced load management.

Features

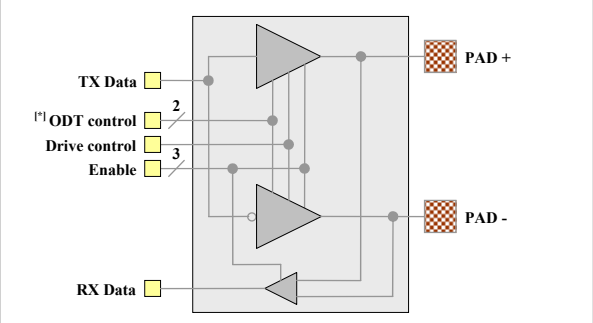
- JEDEC standard compliant
- SSTL_18 with selectable 60% or full drive
- 2.5V FETs
- Up to 400 MHz with balanced load management
- Full complement of pads
- 50Ω, 75Ω and 150Ω termination
- Non-ODT reduced size driver and clock pad (30µm pitch)

SLP_BI_013_18V_D – SSTL_18 Driver



[*] ODT control pins not available in non-ODT pad

SLP_CL_013_18V_D – SSTL_18 Clock Driver



[*] ODT control pins not available in non-ODT pad

Absolute maximum ratings

Parameter	Description	Value	Units
VVDD	Core supply voltage range	-0.5 to 1.4	V
VDVDD	I/O supply voltage range	-0.5 to 2.8	V
VPAD	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V
TA	Storage temperature range	-55 to 150	°C

AC Characteristics

Symbol	Parameter	Max	Unit
F	Max frequency	400	V
P_{DISS}	Power dissipation	15	µW / MHz

Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.90	1.0 to 1.2	1.32	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
V_{VREF}	Reference voltage	0.81	0.9	0.99	V
T_A	Ambient operating temperature	0	25	100	°C
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	0		V_{DVDD}	V
$V_{IH\ (dc)}$	DC input logic high [1]	V_{REF}+125		V_{DVDD}+300	mV
$V_{IL\ (dc)}$	DC input logic low [1]	-300		V_{REF}-125	mV
$V_{IH\ (ac)}$	AC input logic high [1]	V_{REF}+250		-	mV
$V_{IL\ (ac)}$	AC input logic low [1]	-		V_{REF}-250	mV

[1] Single-ended receiver see JEDEC Standard No. 8-15A for more information

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Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.8V	Temperature
1.2 [1]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1 [2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] LP process only.
[2] G process only

Cell summary

Name	Description
SLP_BI_013_18V_D	SSTL_18 driver cell
SLP_CL_013_18V_D	SSTL_18 differential clock cell
SLP_BI_013_18V_D_NOD	SSTL_18 driver cell without ODT
SLP_CL_013_18V_D_NOD	SSTL_18 differential clock cell without ODT
SLP_RE_000_18V	V_{REF} pad
PVP_VD_RCD_12V	Core power pad
PVP_VD_RC2_12V	Double bond core power pad
PVP_VD_RC3_12V	Triple bond core power pad
PVP_VS_RCD_12V	Core ground pad
PVP_VS_RC2_12V	Double bond core ground pad
PVP_VS_RC3_12V	Triple bond core ground pad
PVP_VD_PDO_18V	I/O power pad with POC control
PVP_VD_RDO_18V	I/O power pad without POC control
PVP_VS_RDO_18V	I/O ground supply
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	DVDD, DVSS, POC, BIAS and VREF rail splitter
SPC_AD_SSTL_18V	Adapter to core-limited libraries

Physical size

Name	Width	Height	Units
SLP_BI_013_18V_D	50	200	µm
SLP_CL_013_18V_D	100	200	µm
SLP_BI_013_18V_D_NOD	30	230	µm
SLP_CL_013_18V_D_NOD	60	230	µm
SLP_RE_000_18V	30	180	µm
PVP_VD_RCD_12V	30	180	µm
PVP_VD_RC2_12V	60	180	µm
PVP_VD_RC3_12V	90	180	µm
PVP_VS_RCD_12V	30	180	µm
PVP_VS_RC2_12V	60	180	µm
PVP_VS_RC3_12V	90	180	µm
PVP_VD_PDO_18V	30	180	µm
PVP_VD_RDO_18V	30	180	µm
PVP_VS_RDO_18V	30	180	µm
SVP_SP_000_18V	0.1	180	µm
SVP_SP_001_18V	1	180	µm
SVP_SP_005_18V	5	180	µm
SVP_SP_010_18V	10	180	µm
SPP_RS_005_18V	5	180	µm
SPC_AD_SSTL_18V	5	180	µm

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