CSM65: SSTL_15 Pad Set

Libraries

Name	Process	CUP	Form Factor
RGO_CSM65_18V15_G_30C_SSTL_15	G	yes	staggered
RGO_CSM65_18V15_LP_30C_SSTL_15	LP	yes	staggered
RGO_CSM65_18V15_LPE_30C_SSTL_15	LPE	yes	staggered

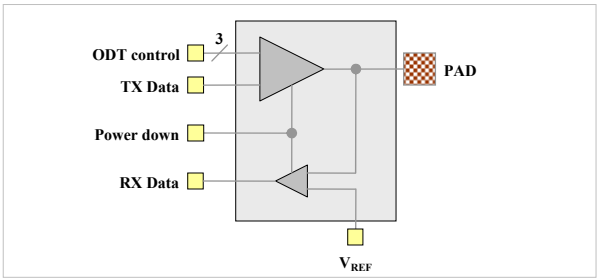
Summary

The SSTL_15 pad set is a full complement of I/O, calibration, power, and spacer cells that are necessary to assemble a padring by abutment. Since the SSTL_15 normally operates with its own isolated power domain (1.5V), a "rail-splitter" support cell (SPP_RS_005_15V) is included to allow the designer to easily break the lines that should not connect to the rest of the padring, while allowing VDD and VSS to be continuous within the padring.

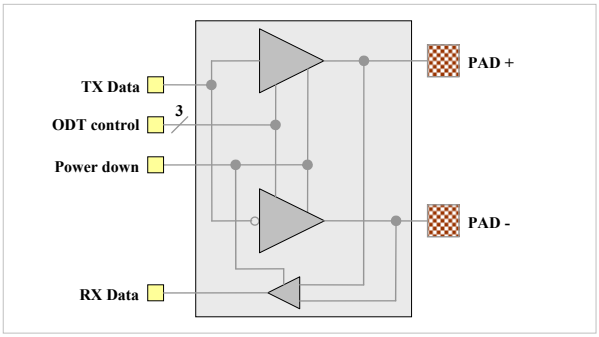
Features

- Full DDR3 capability - 800MHz (1600 Mbps)
- Low Power driving standard DDR3 memories
- 1.8V FETs
- Full complement of cells to build padring (20)
- Full ODT Capability:
  - Either fixed 6-Bit programmation (program from core)
  - Or, dynamic 6-Bit PVT calibration (external reference resistor)

SLP_BI_034_15V_D – SSTL_15 Driver



SLP_CL_034_15V_D – SSTL_15 Clock Driver



Absolute maximum ratings

Parameter	Description	Value	Units
V_{VDD}	Core supply voltage range	-0.5 to 1.4	V
V_{DVDD}	I/O supply voltage range	-0.5 to 2.1	V
V_{PAD}	Voltage range at PAD	-0.5 to (V_{DVDD} + 0.5)	V

Recommended operating conditions

Parameter	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.90	1.0 to 1.2	1.32	V
V_{DVDD}	I/O supply voltage	1.35	1.5	1.65	V
V_{VREF}	Reference voltage	0.81	0.9	0.99	V
T_A	Ambient operating temperature	0	25	100	°C
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	0		V_{DVDD}	V
$V_{IH\ (dc)}$	DC input logic high	V_{REF} + 0.1		TBD	V
$V_{IL\ (dc)}$	DC input logic low	TBD		V_{REF} - 0.1	V
$V_{IH\ (ac)}$	AC input logic high	V_{REF} + 0.175		-	V
$V_{IL\ (ac)}$	AC input logic low	-		V_{REF} - 0.175	V

AC Characteristics

Symbol	Parameter		Max	Unit
F	Max frequency		800	MHz
P_{DISS}	Power dissipation	100 MHz	14.8	mW
		400 MHz	18.2	mW
		800 MHz	22.1	mW

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Characterization Corners

Nominal VDD	Model	VDD	DVDD = 1.5V	Temperature
1.2 [1]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1 [2]	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.0	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] LP & LPE processes.
[2] G process only.

Cell summary

Name	Description
SLP_BI_034_15V_D	SSTL_15 I/O pad
SLP_CL_034_15V_D	Differential clock buffer
SLP_SP_CAL_15V	Calibration pad
SLP_SP_PST_15V	Level shifter cell for pull-up and pull-down turning bits
SLP_RE_000_15V	V_{REF} pad
PVP_VD_RCD_1215V	Core V_{DD} with VREF bus
PVP_VD_RC2_1215V	2x core V_{DD} with VREF bus
PVP_VD_RC3_1215V	3x core V_{DD} with VREF bus
PVP_VS_RCD_1215V	Core V_{SS} pad with VREF bus
PVP_VS_RC2_1215V	2x core V_{SS} pad with VREF bus
PVP_VS_RC3_1215V	3x core V_{SS} pad with VREF bus
PVP_VD_PDO_15V	I/O V_{DD} pad with POC control
PVP_VD_RDO_15V	I/O V_{DD} pad without POC control
PVP_VS_RDO_15V	I/O V_{SS} with VREF bus
SVP_SP_000_15V	0.1 µm spacer
SVP_SP_001_15V	1 µm spacer
SVP_SP_005_15V	5 µm spacer
SVP_SP_020_15V	20 µm spacer
SPP_RS_005_15V	DVDD, DVSS, POC, CP[1..3], CN[1..3] and VREF rail splitter
SPP_AD_SSTL_15V	Adapter to staggered libraries

Physical size

Name	Width	Height	Units
SLP_BI_034_15V_D	40	255	µm
SLP_CL_034_15V_D	80	255	µm
SLP_SP_CAL_15V	60	300	µm
SLP_SP_PST_15V	30	255	µm
SLP_RE_000_15V	30	255	µm
PVP_VD_RCD_1215V	30	255	µm
PVP_VD_RC2_1215V	60	255	µm
PVP_VD_RC3_1215V	90	255	µm
PVP_VS_RCD_1215V	30	255	µm
PVP_VS_RC2_1215V	60	255	µm
PVP_VS_RC3_1215V	90	255	µm
PVP_VD_PDO_15V	30	255	µm
PVP_VD_RDO_15V	30	255	µm
PVP_VS_RDO_15V	30	255	µm
SVP_SP_000_15V	0.1	255	µm
SVP_SP_001_15V	1	255	µm
SVP_SP_005_15V	5	255	µm
SVP_SP_020_15V	20	255	µm
SPP_RS_005_15V	5	255	µm
SPP_AD_SSTL_15V	25	255	µm

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