TSMC 16/12: (R)GMII

Libraries

Name	Process	Form Factor
RGO_TSMC16_18V33_FFC_20C_RGMII	FFC	Staggered CUP
RGO_TSMC12_18V33_FFC_LL_20C_RGMII	FFC_LL	Staggered CUP

Summary

The (R)GMII library provides the combo driver / receiver cell for both Gigabit Media Independent Interface signaling and Reduced Gigabit Media Independent Interface signaling. It is designed to interface Ethernet PHY to network switch ASICs. It is compliant with IEEE 802.2-2005 (GMII) and HP RGMII, version 1.3, 12/10/2000.

These libraries are offered at both 16nm and a 12nm shrink. They are available in a staggered CUP wire bond implementation with a flip chip option.

To utilize these cells in the pad ring, an additional library is required – 3.3V Support: Power. That library contains the necessary power cells, the POC and VREF cells, and a rail splitter to isolate the (R)GMII cells in their own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.
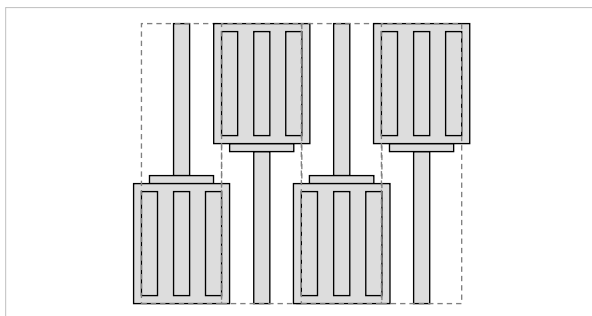
ESD Protection:
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
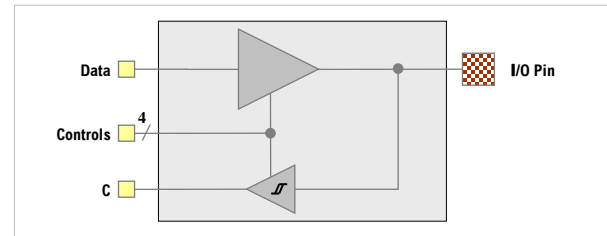 - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 64.416μm x 220.032μm

MIP_BI_SDS_33V_NC

(R)GMII Combo Driver Features:

- Selectable output slew rate
- GMII mode powered by 3.3V I/O & 0.8V core supplies
- 2.5V RGMII mode powered by 2.5V I/O & 0.8V core supplies
- 1.8V RGMII mode powered by 2.5V I/O & 0.8V core supplies

Vertical-only (_V) and and horizontal-only (_H) variants provided.

Recommended operating conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.72	0.80	0.88	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at IO		0		V_{DVDD}	V
V_{DVDD}	I/O supply voltage		2.97	3.3	3.63	V
V_{IH}	Input logic high	GMII	1.7	-	-	V
V_{IL}	Input logic low		-	-	0.9	V
V_{IL_AC}	Input high voltage, AC		1.9	-	-	V
V_{IH_AC}	Input low voltage, AC		-	-	0.7	V
V_{OH}	Output logic high voltage		2.1	-	3.6	V
V_{OL}	Output logic low voltage		0	-	0.5	V
V_{DVDD}	I/O supply voltage		2.25	2.5	2.75	V
V_{IH}	Input logic high	2.5V RGMII	1.7	-	-	V
V_{IL}	Input logic low		-	-	0.7	V
V_{OH}	Output logic high voltage		2.0	-	V_{DVDD} +0.3	V
V_{OL}	Output logic low voltage		V_{DVSS} - 0.3	-	0.4	V
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
V_{IH}	Input logic high	1.8V RGMII	0.7 x V_{DVDD}	-	-	V
V_{IL}	Input logic low		-	-	0.3 x V_{DVDD}	V
V_{OH}	Output logic high voltage		2.0	-	V_{DVDD} +0.3	V
V_{OL}	Output logic low voltage		V_{DVSS} - 0.3	-	0.4	V

[1] The lowest supported frequency is 10BASE-T over RGMII

Characterization Corners (16nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V, 3.3V

Characterization Corners (12nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V, 3.3V