TSMC 16/12: RF

Libraries

Name	Process	Form Factor
RGO_TSMC16_18V33_FFC_40C_RF	FFC	Inline CUP
RGO_TSMC12_18V33_FFC_LL_40C_RF	FFC_LL	Inline CUP

Summary

The RF library provides Analog / RF I/O cells including LNA input pads, a 5V tolerant PA output pad and a 10GHz analog signal pad with multiple input resistance options. Discrete components (RF diodes and SCR's) are provided to enable construction of a custom ESD protection solution.

These libraries are offered at both 16nm and a 12nm shrink. They are available in an inline CUP wire bond implementation with a flip chip option.

ESD Protection:

- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

RF Diodes

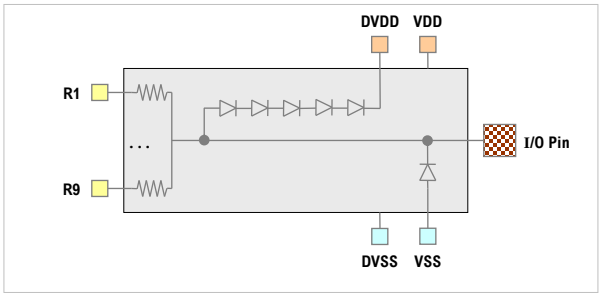
A set of PPLUS_NWELL_DIODE RF diodes provide minimum capacitance for RF applications and high current handling capability for good ESD protection.

Silicon-Controlled Rectifiers (SCR)

A set of P+ to Nwell SCR discrete components provide the lowest capacitance with the highest ESD protection. These components have been used in I/O pads to demonstrate over 6KV ESD protection.

ANP_BI_DWR_5T

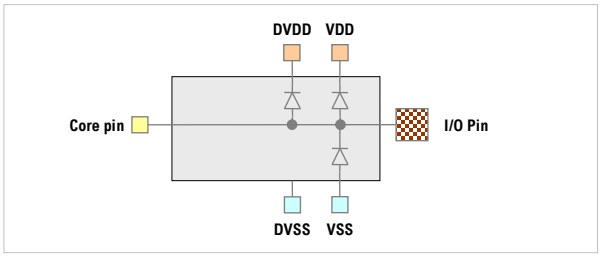
ANP_BI_DWR_5T is a bi-directional analog signal pad with selectable input resistance. Resistors R1 to R4 and R6 to R9 can be used in parallel to achieve the desired resistance value as low as 1.3 ohms.
This structure can then be used with output amplifiers for which R5 can be used in the feedback path. If used in this manner, R1 to R4 and R6 to R9 should be individually connected to isolated fingers of the driver transistors.



Analog / RF Pads

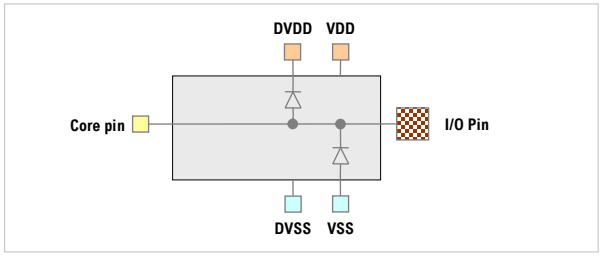
ANP_IN_LNA_1033V

ANP_IN_LNA_10V is a 0 to 0.8V analog I/O pad optimized for low capacitance and designed to protect thin gate oxide input devices. The layout uses wide metal 3 interconnect (14 µm) for low inductance from the bond pad to the core. Additional variants (_UVT & _OVT) provide lower capacitance and the ability to handle occasional signal undershoot / overshoot of 0.7V.



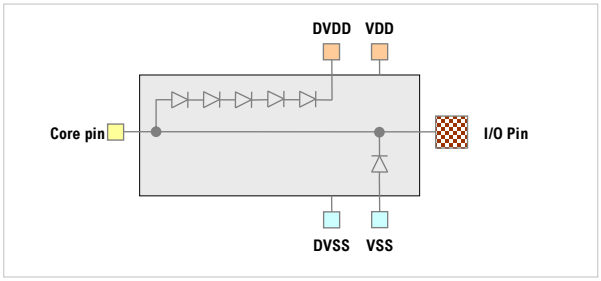
ANP_IN_LNA_33V

ANP_IN_LNA_33V is a 0 to 3.3V analog I/O pad optimized for low capacitance. The layout uses wide metal 3 interconnect (12 µm) for low inductance from the bond pad to the core.



ANP_OU_PWA_5T

ANP_OU_PWA_5T is an analog I/O pad optimized for low capacitance which uses SCRs for ESD clamp devices.
The stacked diode ESD structure from DVDD to the I/O pin provides extended overvoltage protection. With a 3.3V power supply, this I/O pad is 5V tolerant. Dropping to an I/O domain power supply of 1.8V, the pad is 3.3V tolerant.



Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.72	0.80	0.88	V
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
		1.08	1.2	1.32	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

Characterization Corners (16nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.8V, 2.5V & 3.3V

Characterization Corners (12nm)

Model	LPE Type	VDD=0.8V	DVDD [1]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] DVDD = 1.2V, 1.8V, 2.5V & 3.3V

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