## **TSMC 16/12: LVDS**



#### Libraries

Name	Process	Form Factor
RGO_TSMC16_18V25_FFC_UC_LVDS	FFC	Staggered CUP
RG0_TSMC12_18V25_FFC_LL_UC_LVDS	FFC_LL	Staggered CUP

#### Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 2.4 Gbps. Also included is a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

These libraries are offered at both 16nm and a 12nm shrink. They are available in a staggered CUP wire bond implementation with a flip chip option.

#### LVDS Specification Compliant:

- TIA/EIA-644-A Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

#### **ESD Protection:**

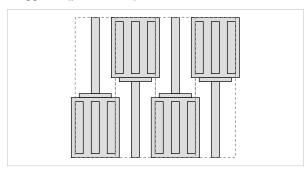
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - o 500 V ESD Charge Device Model (CDM)

#### Latch-up Immunity:

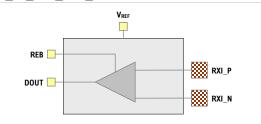
- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100$ mA @ 125°C

#### **Cell Size & Form Factor**

#### Staggered (pad-limited) – 50.4 $\mu$ m x 165.024 $\mu$ m



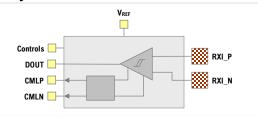
#### LDP\_IN\_800\_25V\_DN: 2.0GHz LVDS Receiver



#### LVDS Receiver Features:

- Operates up to 2.0 GHz (4.0 Gbps)
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Duty Cycle Distortion (DCD) 50 ps typical
- Common mode range from 0V to 2.4V (limited by power supply)
- Powered by 1.8V I/O and 0.8V core supplies

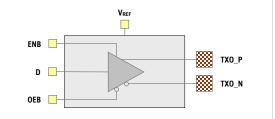
### LDP\_IN\_800\_25V\_DS: 1.2GHz LVDS Receiver with hysteresis and CML out



#### LVDS Receiver Features:

- DOUT operates up to 1.2 GHz (2.4 Gbps)
- CML Out operates up to 800 MHz (1.6 Gbps)
- Input receive sensitivity of 100mV with hysteresis and 75mV without hysteresis (peak differential)
- Duty Cycle Distortion (DCD) 50 ps typical
- Common mode range from 0V to 2.4V (limited by power supply)
- Powered by 1.8V I/O and 0.8V core supplies

#### LDP\_OU\_800\_18V\_T: 2.0GHz LVDS Driver



#### LVDS Driver Features:

- Operates up to 2.0 GHz (4.0 Gbps) with external 1 pF load
- Common mode output range 1.1V ±100mV
- Supports single termination (far end) only  $-100\Omega$  differential
- Powered by 1.8V I/O and 0.8V core supplies

## **TSMC 16/12: LVDS**



#### **Recommended operating conditions**

Symbo	Description	Min	Nom	Max	Units
VVDD	Core supply voltage	0.72	0.80	0.88	V
Vdvdd	I/O supply voltage	1.62	1.8	1.98	V
TJ	Junction temperature	-40	25	125	°C
VPAD	Voltage at PAD	-0.3V		V <sub>DVDD</sub> +0.3V	V
VIH	Input high at PAD	0.7 * V <sub>DVDD</sub>		V <sub>DVDD</sub> + 0.3	V
VIL	Input low at PAD	V <sub>DVSS</sub> - 0.3		0.3 * V <sub>DVDD</sub>	V

#### **Characterization Corners (16nm)**

Model	LPE Type	VDD=0.8V	DVDD=1.8V	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

#### **Characterization Corners (12nm)**

Model	LPE Type	VDD=0.8V	DVDD=1.8V	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

#### **Cell Summary & Physical Sizes**

Name	Description
LDP_IN_800_25V_DN *	2.0 GHz LVDS input cell
LDP_IN_800_25V_DS *	1.2 GHz LVDS input cell
LDP_OU_800_18V_T *	2.0 GHz LVDS output cell
LDP_RE_000_18V *	LVDS Voltage Reference cell
PVP_VD_RCD_10V	Core power (VDD)
PVP_VS_RCD_10V	Core ground (VSS)
PVP_VD_PDO_18V *	I/O power (DVDD) with POC control
PVP_VD_RDO_18V	I/O power (DVDD)
PVP_VS_RDO_18V	I/O ground (VSS)
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	Rail splitter

\*Supplied in vertical-only and horizontal-only orientations

# Staggered CUP Cells CUP\_TSMC16\_44X80\_IN 44µm X 80µm Inner CUP\_TSMC16\_44X80\_OUT 44µm X 80µm Outer CUP\_TSMC16\_FC Flip chip with top metal port CUP\_TSMC16\_FC\_NRV Flip chip without RV vias

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