TSMC 16/12: 1.8V 100MHz Oscillators

Libraries

Name	Process	Form Factor
RGO_TSMC16_18V18_FFC_20C_OSC	FFC	Staggered CUP
RGO_TSMC12_18V18_FFC_LL_20C_OSC	FFC_LL	Staggered CUP

Summary

The 1.8V 100MHz Oscillators library includes a programmable oscillator macro I/O cell.

- 100 MHz programmable oscillator

These libraries are offered at both 16nm and a 12nm shrink. They are available in a staggered CUP wire bond implementation with a flip chip option.

To utilize these cells in the pad ring, an additional library is required – 1.8V Support: Power. That library contains the DVDD/DVSS power cells necessary for ESD protection, the POC cell, and a rail splitter to isolate the oscillator in its own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

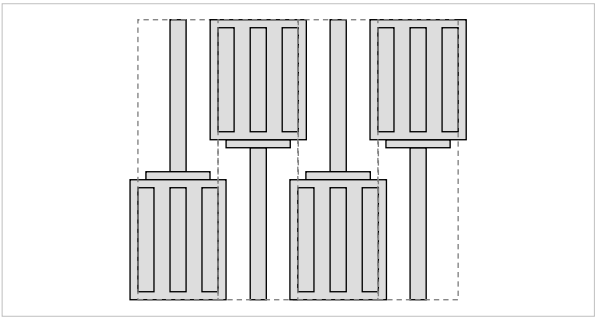
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

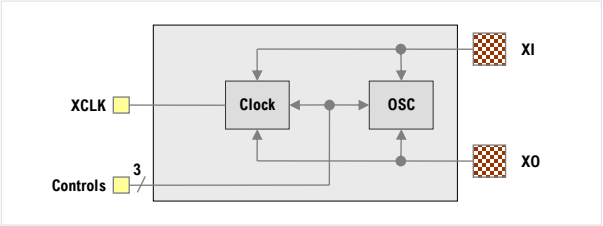
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 100.8µm x 165.024µm



OSP_BI_100_18V



100 MHz Programmable Oscillator Features

- Programmable drive strength for wider frequency range – 1 MHz to 100 MHz using industry standard external crystals.
- Optimized for stability and minimum jitter
- Power-down mode
- Operates on core power only (VDD/VSS cells embedded)
- In a forced bypass mode, the XI port can be driven by an I/O-level (V_{DVDD}) clock signal.

Vertical-only (_V) and and horizontal-only (_H) variants provided.

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.72	0.80	0.88	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at XI [1]	0	-	V_{DVDD}	V

[1] XI can be driven by an external clock for bypass operation. XO should never be driven or loaded by anything other than the oscillator crystal.

Characterization Corners (16nm)

Model	LPE Type	VDD=0.8V	DVDD=1.8V	Temp
FFGNP	Cbest_CCbest_T	+10%	+10%	-40°C
FFGNP	Cbest_CCbest_T	+10%	+10%	0°C
FFGNP	Cbest_CCbest_T	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst_T	-10%	-10%	-40°C
SSGNP	Cworst_CCworst_T	-10%	-10%	0°C
SSGNP	Cworst_CCworst_T	-10%	-10%	125°C

Characterization Corners (12nm)

Model	LPE Type	VDD=0.8V	DVDD=1.8V	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

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