SMG28: SD

Libraries

Name	Process	Form Factor
RGO_SMG28_18V33_FDS_20C_SD	FD-SOI	Staggered CUP

Summary

The SD library provides a bidirectional SD 3.0 signaling cell. It is compatible with revision 3.01 of the SD Specifications, Part 1, Physical Layer Specification. This library is offered as a supplement to the standard GPIO libraries provided by Aragio Solutions.

This 28nm library is available in a staggered CUP wire bond implementation.

To utilize this cell in the pad ring, an additional library is required – 3.3V Support: Power. That library contains the necessary power cells, the POC and VREF cells, and a rail splitter to isolate the SD cells in their own power domain if desired. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a complete pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

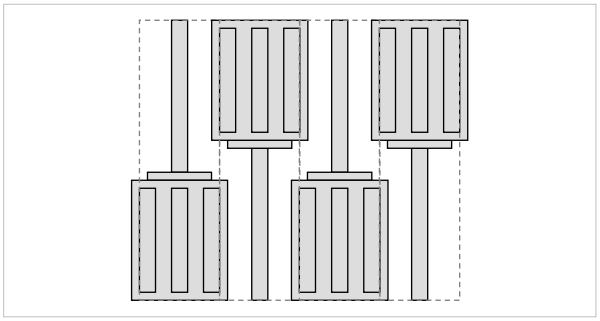
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

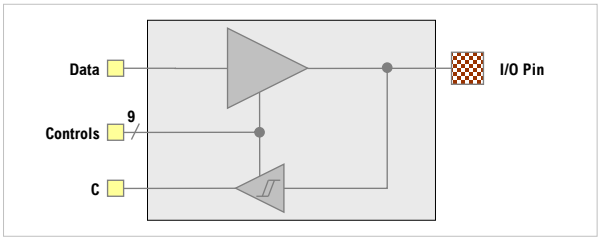
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 35µm x 140µm



STP_BI_016_1833V_SD3



Bidirectional SD 3.0 Driver Features

- Dual voltage operation (1.8V & 3.3V)
- Programmable drive strength
- Selectable output slew-rate (slow / fast)
- Selectable schmitt trigger input
- Programmable input options (pull-up, pull-down, or hi-Z)
- Fully compatible with Aragio Solutions 3.3V I/O library offerings
- Power-up sequencing independent design with Power-on Control

Recommended operating conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.9	1.0	1.1	V
			0.99	1.1	1.155	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at IO		-0.3		V_{DVDD} + 0.3	V
V_{DVDD}	I/O supply voltage		2.7	3.3	3.63	V
V_{IH}	Input logic high	3.3V	0.625 * V_{DVDD}	-	V_{DVDD} + 0.3	V
V_{IL}	Input logic low	3.3V	V_{DVSS} - 0.3	-	0.25 * V_{DVDD}	V
V_{HYS}[1]	Input hysteresis voltage		0.2	-	-	V
V_{DVDD}	I/O supply voltage		1.7	1.8	1.95	V
V_{IH}	Input logic high	1.8V	0.65 * V_{DVDD}	-	V_{DVDD} + 0.3	V
V_{IL}	Input logic low	1.8V	V_{DVSS} - 0.3	-	0.35 * V_{DVDD}	V
V_{HYS} [1]	Input hysteresis voltage		0.1 * V_{DVDD}	-	-	V

[1] When SMT = 1.

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
1.0V	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	FF	+10%	+10%	85°C
	FF	+10%	+10%	0°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1V Overdrive	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	FF	+5%	+10%	85°C
	FF	+5%	+10%	0°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] DVDD = 1.8V, 3.0V & 3.3V

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