SMG28: LVDS

Libraries

Name	Process	Form Factor
RGO_SMG28_18V25_FDS_UC_LVDS	FD-SOI	Staggered CUP

Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 2.4 Gbps. Also included is a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

This 28nm library is available in a staggered CUP wire bond implementation.

LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

ESD Protection:

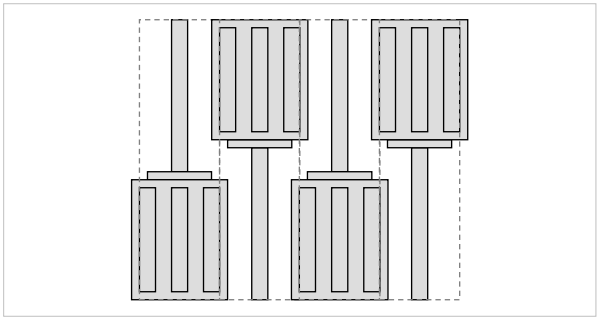
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

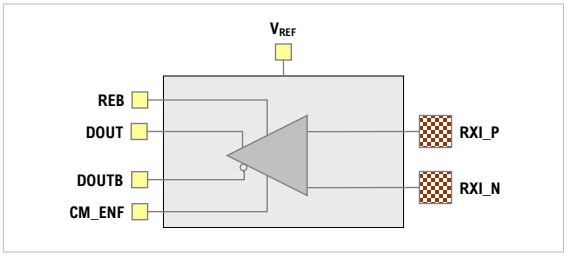
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 50µm x 129µm



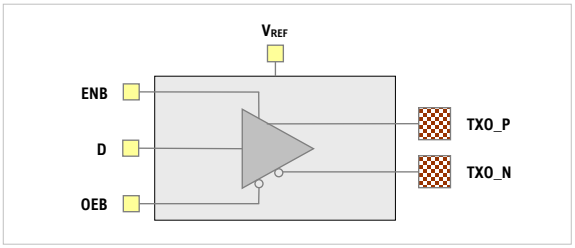
LDP_IN_800_25V_DN: 1.2GHz LVDS Receiver



LVDS Receiver Features:

- Operates up to 1.2 GHz (2.4 Gbps)
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Duty Cycle Distortion (DCD) – 50 ps typical
- Common mode range from 0V to 1.8V (limited by power supply)
- Common mode enforcement option

LDP_OU_800_18V_T: 1.0GHz LVDS Driver



LVDS Driver Features:

- Operates up to 1.0 GHz (2.0 Gbps) with external 1 pF load
- Common mode output range 1.1V ±100mV
- Supports single termination (far end) only – 100Ω differential

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.9	1.0	1.1	V
		0.99	1.1	1.155	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V
V_{IH}	Input high at PAD	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Input low at PAD	V_{DVSS} - 0.3		0.3 * V_{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
1.0V	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	FF	+10%	+10%	85°C
	FF	+10%	+10%	0°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C
1.1V Overdrive	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	FF	+5%	+10%	85°C
	FF	+5%	+10%	0°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] DVDD = 1.8V

Cell Summary & Physical Sizes

Name	Description
LDP_IN_800_25V_DN	1.2 GHz LVDS input cell
LDP_OU_800_18V_T	1.0 GHz LVDS output cell
LDP_RE_000_18V	LVDS Voltage Reference cell
PVP_VD_RCD_10V	Core power (VDD)
PVP_VS_RCD_10V	Core ground (VSS)
PVP_VD_PDO_18V	I/O power (DVDD) with POC control
PVP_VD_RDO_18V	I/O power (DVDD)
PVP_VS_RDO_18V	I/O ground (VSS)
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	Rail splitter

Staggered CUP Cells	
CUP_SMG28_85X55_IN	85µm X 55µm Inner
CUP_SMG28_85X55_OUT	85µm X 55µm Outer

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