

## Libraries

Name	Process	Form Factor
RGO_SMG28_18V25_FDS_UC_LVDS	FD-SOI	Staggered CUP

## Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 2.4 Gbps. Also included is a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

This 28nm library is available in a staggered CUP wire bond implementation.

### LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

### ESD Protection:

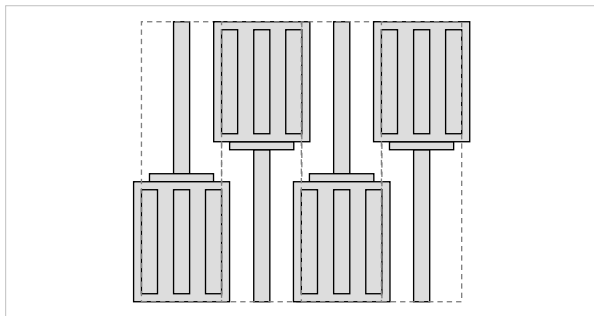
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

### Latch-up Immunity:

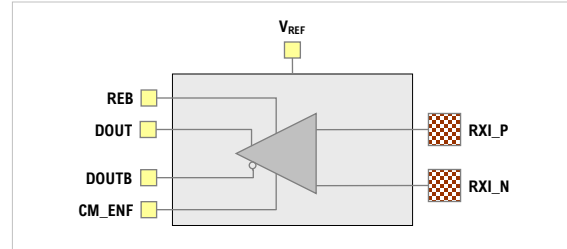
- JEDEC compliant
  - Tested to I-Test criteria of  $\pm 100\text{mA}$  @  $125^\circ\text{C}$

## Cell Size & Form Factor

Staggered (pad-limited) –  $50\mu\text{m} \times 129\mu\text{m}$



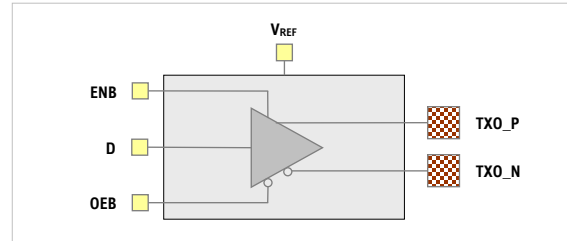
## LDP\_IN\_800\_25V\_DN: 1.2GHz LVDS Receiver



### LVDS Receiver Features:

- Operates up to 1.2 GHz (2.4 Gbps)
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Duty Cycle Distortion (DCD) – 50 ps typical
- Common mode range from 0V to 1.8V (limited by power supply)
- Common mode enforcement option

## LDP\_OU\_800\_18V\_T: 1.0GHz LVDS Driver



### LVDS Driver Features:

- Operates up to 1.0 GHz (2.0 Gbps) with external 1 pF load
- Common mode output range  $1.1\text{V} \pm 100\text{mV}$
- Supports single termination (far end) only –  $100\Omega$  differential

## Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V <sub>VDD</sub>	Core supply voltage	0.9	1.0	1.1	V
		0.99	1.1	1.155	V
V <sub>DVDD</sub>	I/O supply voltage	1.62	1.8	1.98	V
T <sub>J</sub>	Junction temperature	-40	25	125	°C
V <sub>PAD</sub>	Voltage at PAD	-0.3V		V <sub>DVDD</sub> +0.3V	V
V <sub>IH</sub>	Input high at PAD	0.7 * V <sub>DVDD</sub>		V <sub>DVDD</sub> + 0.3	V
V <sub>IL</sub>	Input low at PAD	V <sub>DVSS</sub> - 0.3		0.3 * V <sub>DVDD</sub>	V

## Characterization Corners

Nominal VDD	Model	VDD	DVDD <sup>[1]</sup>	Temperature
1.0V	FF	+10%	+10%	-40°C
	FF	+10%	+10%	125°C
	FF	+10%	+10%	85°C
	FF	+10%	+10%	0°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	85°C
	SS	-10%	-10%	-40°C
1.1V Overdrive	FF	+5%	+10%	-40°C
	FF	+5%	+10%	125°C
	FF	+5%	+10%	85°C
	FF	+5%	+10%	0°C
	TT	nominal	nominal	25°C
	SS	-10%	-10%	0°C
	SS	-10%	-10%	85°C
	SS	-10%	-10%	-40°C
	SS	-10%	-10%	125°C

[1] DVDD = 1.8V

## Cell Summary & Physical Sizes

Name	Description
LDP_IN_800_25V_DN	1.2 GHz LVDS input cell
LDP_OU_800_18V_T	1.0 GHz LVDS output cell
LDP_RE_000_18V	LVDS Voltage Reference cell
PVP_VD_RCD_10V	Core power (VDD)
PVP_VS_RCD_10V	Core ground (VSS)
PVP_VD_PDO_18V	I/O power (DVDD) with POC control
PVP_VD_RDO_18V	I/O power (DVDD)
PVP_VS_RDO_18V	I/O ground (VSS)
SVP_SP_000_18V	0.1 μm spacer
SVP_SP_001_18V	1 μm spacer
SVP_SP_005_18V	5 μm spacer
SVP_SP_010_18V	10 μm spacer
SPP_RS_005_18V	Rail splitter

## Staggered CUP Cells

CUP_SMG28_85X55_IN	85μm X 55μm Inner
CUP_SMG28_85X55_OUT	85μm X 55μm Outer

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