SMIC28: 3.3V Support: Power

Libraries

Name	Process	Form Factor
RGO_SMIC28_18V33_HKCP_20C_SPT	HKC+	Staggered CUP
RGO_SMIC28_18V33_HKCP_40C_SPT	HKC+	Inline CUP

Summary

The 3.3V Support: Power library provides a full complement of cells to support the assembly of a complete pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

These 28nm libraries are available in inline and staggered CUP wire bond implementations with a flip chip option.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

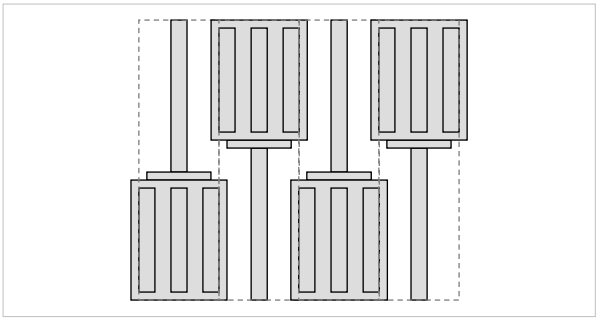
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

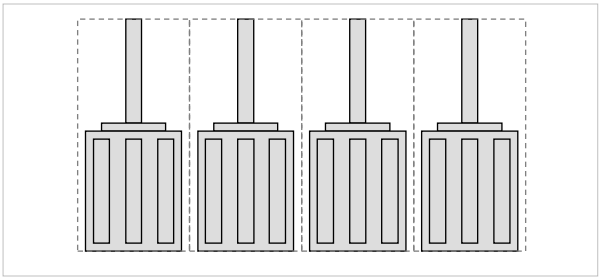
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 25µm x 165µm



Inline (core-limited) – 45µm x 100µm



Cell List

Name	Description
Digital Pads	
STx_IN_001_33V_NC *	Input-only buffer
I/O Power / Ground Pads	
PWx_VD_RDO_33V	I/O power (DVDD)
PWx_VS_RDO_33V	I/O ground (DVSS)
Core Power / Ground Pads	
PWx_VD_RCD_1033V	Core power (VDD)
PWx_VS_RCD_1033V	Core ground (VSS)
Analog Pads	
ANx_BI_DWR_33V	Analog Input cell
Analog Power / Ground Pads	
PWx_VD_ANA_1033V	Analog power (AVDD) 1.0V
PWx_VS_ANA_1033V	Analog ground (AVSS)
PWx_VD_ANA_33V	Analog power (ADVDD) 3.3V
PWx_VS_ANA_33V	Analog ground (ADVSS)
Support Pads	
SPx_CO_000_33V	Corner cell (rail splitter)
SPx_CO_001_33V	Corner cell (continuous)
SPx_SP_000_33V	0.1µm spacer
SPx_SP_001_33V	1µm spacer
SPx_SP_005_33V	5µm spacer
SPx_SP_010_33V	10µm spacer
SPx_RS_005_33V	Rail splitter
SPx_RE_SVR_182533V	VREF generation
SPx_SP_POC_1833V *	POC / HVPS generation

* Vertical-only (_V) and horizontal only(_H) variants provided
Cell names / descriptions abbreviated

Staggered CUP Cells	
CUP_SMIC28_44X80_IN	44µm X 80µm Inner
CUP_SMIC28_44X80_OUT	44µm X 80µm Outer
CUP_SMIC28_46P7X80_IN	46.7µm X 80µm Inner
CUP_SMIC28_46P7X80_OUT	46.7µm X 80µm Outer
CUP_SMIC28_48X48_IN	48µm X 48µm Inner
CUP_SMIC28_48X48_OUT	48µm X 48µm Outer
CUP_SMIC28_48X63_IN	48µm X 63µm Inner
CUP_SMIC28_48X63_OUT	48µm X 63µm Outer
CUP_SMIC28_33V_FC	Flip chip with top metal port
CUP_SMIC28_33V_FC_NRV	Flip chip without RV via

Inline CUP Cells	
CUP_SMIC28_40X80_INLINE	40µm X 80 µm Inline
CUP_SMIC28_44X80_INLINE	44µm X 80 µm Inline
CUP_SMIC28_48P9X80_INLINE	48.9µm X 80 µm Inline
CUP_SMIC28_50X50_INLINE	50µm X 50 µm Inline
CUP_SMIC28_INLINE_FC	Flip chip with top metal port

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.90	0.99	V
V_{DVDD}	I/O supply voltage	2.97	3.3	3.63	V
		2.25	2.5	2.75	V
		1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

Characterization Corners

Model	LPE Type	VDD=0.9V	DVDD [1]	Temp
FFG	Cbest	+10%	+10%	-40°C
FFG	Cbest	+10%	+10%	0°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSG	Cworst	-10%	-10%	-40°C
SSG	Cworst	-10%	-10%	0
SSG	Cworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 2.5V & 3.3V

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