TSMC22: SD

Libraries

Name	Process	Form Factor
RGO_TSMC22_18V33_ULP_20C_SD3	ULP	Staggered CUP

Summary

The SD library provides bidirectional SD 3.0 signaling cells. It is compliant with the SD Specifications, Part 1, Physical Layer Specification (Revision 3.01, February 18, 2010).

This library is available in a staggered CUP wire bond implementation with a flip chip option.

To design an operational I/O power domain with these cells, an additional library is required – 3.3V Wide Range GPIO. That library contains a full complement of cells to support the assembly of a functional pad ring by abutment. That set includes an input-only buffer, isolated analog I/O, and power / ground cells along with corner and spacer cells. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

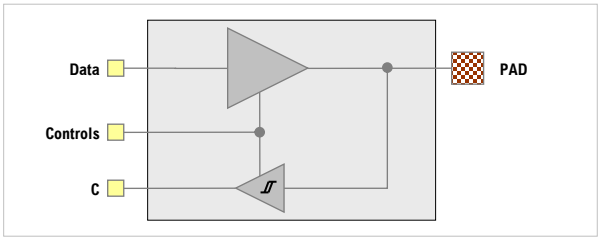
- Staggered (pad-limited)
  - SD3 – 36µm x 165µm
  - VREF – 25µm x 165µm

Characterization Corners

Nom VDD	Model	LPE	VDD	DVDD [1]	Temp
0.9V	FF	Cbest	+10%	+10%	-40°C
	FF	Cbest	+10%	+10%	0°C
	FF	Cbest	+10%	+10%	125°C
	FFG	Ctypical	+10%	+10%	125°C
	TT	Ctypical	nominal	nominal	25°C
	TT	Ctypical	nominal	nominal	85°C
	SS	Cworst	-10%	-10%	-40°C
	SS	Cworst	-10%	-10%	0°C
	SS	Cworst	-10%	-10%	125°C

[1] DVDD = 1.8V, 3.3V

STP_BI_016_1833V_SD3



Bidirectional SD 3.0 Driver Features

- Dual voltage operation (1.8V & 3.3V)
- Programmable drive strength
- Selectable output slew-rate (slow / fast)
- Selectable Schmitt trigger input
- Programmable input options (hi-Z/pull-up/pull-down)
- Fully compatible with Aragio Solutions 3.3V I/O library offerings
- Power-up sequencing independent design with Power-on Control

For proper operation, the **SPP_RE_SDVR_1833V** voltage reference cell, included in this library, is required in the SD power domain.

Recommended Operating Conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.81	0.9	0.99	V
T_J	Junction temp		-40	25	+125	°C
V_{PAD}	Voltage at IO		-0.3		V_{DVDD}+0.3	V
V_{DVDD}	I/O supply voltage	3.3V	2.7	3.3	3.63	V
V_{IH}	Input logic high	3.3V	0.625*V_{DVDD}	-	V_{DVDD}+0.3	V
V_{IL}	Input logic low	3.3V	V_{DVSS} - 0.3	-	0.25*V_{DVDD}	V
V_{HYS}[1]	Input hysteresis	3.3V	0.2	-	1.4	V
V_{DVDD}	I/O supply voltage	1.8V	1.7	1.8	1.95	V
V_{IH}	Input logic high	1.8V	1.27	-	2.0	V
V_{IL}	Input logic low	1.8V	V_{DVSS} - 0.3	-	0.58	V
V_{HYS} [1]	Input hysteresis	1.8V	0.1 * V_{DVDD}	-	0.4*V_{DVDD}	V

[1] When SMT = 1.

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