TSMC 06/07: I2C

Libraries

Name	Process	Form Factor
RGO_TSMC06_18V33_6FF_20F_I2C	6FF	Staggered Flip Chip
RGO_TSMC07_18V33_7FF_20C_I2C	7FF	Staggered Flip Chip

Summary

The I2C library provides open-drain bi-directional I/O cells designed for the I²C two-line interface. It is compliant with the I²C-bus specification – UMC10204 I²C-bus specification and user manual, Rev.4 – 13 February 2012, NXP.

The design supports the Sm, Fm and Hs modes of operation at the I²C bus operating voltage (VDDP) of either extended range 3.3V or standard 1.8V logic.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

To utilize these cells in the pad ring, an additional library is required – 1.8V Support: Power. That library contains the power cells, the POC cell, and a rail splitter to isolate the I2C cells in their own power domain as recommended. It also contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a functional pad ring by abutment. The rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

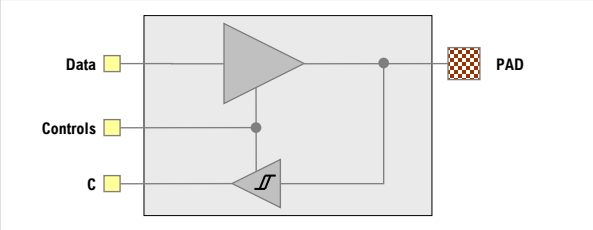
Cell Size & Form Factor

- Staggered (pad-limited) – 34.08µm x 213µm
- Flip chip implementation with CUP structure built in

Recommended Operating Conditions

	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.675	0.75	0.825	V
V_{DVDD}	I/O supply voltage		1.62	1.8	1.98	V
V_{VDDP}	External pull-up to PAD	3.3V	2.70	3.3	3.63	V
		1.8V	1.62	1.8	1.98	V
T_J	Junction temperature		-40	25	125	°C
V_{PAD}	Voltage at PAD		V_{DVSS} – 0.3	-	3.63	V

I2P_ON_003_1833V_NC



I²C Bi-directional Driver Features

- Supported I²C operating modes:
  - Standard-mode (Sm) – 100 Kbps data rate
  - Fast mode (Fm) – 400 Kbps data rate
  - High speed mode (Hs) – 3.4 Mbps data rate
- Open drain operation only
- Built-in output slew rate control to meet I²C T_{of} minimum of (20 x VDDP/5.5V) ns
- Output enable
- Receiver enable
- ESD protection is accomplished with snapback devices
- Standard LVCMOS compatible inputs with Schmitt trigger (hysteresis) option
- Power-on sequencing independent design with Power-On Control
- DVDD = 1.62V to 1.98V
- Pad VDDP (power supply reference for Output)
  - 2.7V to 3.63V – extended range 3.3V
  - 1.62V to 1.98V – standard range 1.8V
- The circuit consumes no DC supply current in the static state

An open-drain design, this cell requires an external pull-up resistor to a high voltage power supply. The pull-up power supply (VDDP) can be 3.63V maximum, independent of the I/O cell power supply (DVDD). In a 1.8V I2C bus application, VDDP can track DVDD but it is not necessary. The sizing of the external resistor or appropriate pull-up network is application dependent.

Characterization Corners

Model [1]	LPE Type	VDD=0.75V	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.
[2] DVDD = 1.8V, 3.0V & 3.3V

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