TSMC 06/07: LVDS

Libraries

Name	Process	Form Factor
RGO_TSMC06_18V25_6FF_UF_LVDS	6FF	Staggered Flip Chip
RGO_TSMC07_18V25_7FF_UC_LVDS	7FF	Staggered Flip Chip

Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 4.0 Gbps.

LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

Additionally, this library provides a full complement of cells to support the assembly of a functional pad ring by abutment.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

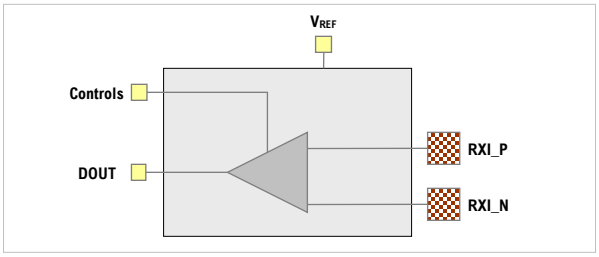
Cell Size & Form Factor

- Staggered (pad-limited) – 46.38µm x 191.28µm
- Flip chip implementation with CUP structure built in

Recommended Operating Conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.675	0.75	0.825	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V

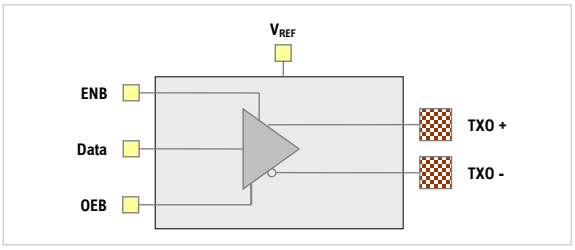
LDP_IN_800_25V_DN: 2.0 GHz LVDS Receiver



LVDS Receiver Features:

- Operates up to 2.0 GHz (4.0 Gbps)
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Common mode range from 0V to 2.4V (limited by power supply)
- Low power consumption

LDP_OU_800_18V_T: 2.0 GHz LVDS Driver



LVDS Driver Features:

- Operates up to 2.0 GHz (4.0 Gbps) with external 1pF load
- Common mode output range 1.1V ±100mV
- Supports 100Ω differential terminations – single ended
- Low power consumption

Characterization Corners

Model [1]	LPE Type	VDD= 0.75V	DVDD=1.8V	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	o°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C
SS	Cworst_CCworst	-10%	-10%	125°C

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.

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Cell Summary

Name	Description
LDP_IN_800_25V_DN	LVDS receiver cell
LDP_OU_800_18V_T	LVDS driver cell
LDP_RE_000_18V	LVDS Voltage Reference cell
PVP_VD_RCD_10V	Core power (VDD)
PVP_VS_RCD_10V	Core ground (VSS)
PVP_VD_PDO_18V	I/O power (DVDD) with POC
PVP_VD_RDO_18V	I/O power (DVDD)
PVP_VS_RDO_18V	I/O ground (VSS)
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	Rail splitter

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