TSMC 06/07: 1.8V GPIO

Libraries

Name	Process	Form Factor
RGO_TSMC06_18V18_6FF_20F	6FF	Staggered Flip Chip
RGO_TSMC07_18V18_7FF_20C	7FF	Staggered Flip Chip

Summary

The 1.8V GPIO library provides general purpose bidirectional I/O cells. These programmable, multi-voltage I/O's give the system designer the flexibility to design to a wide range of performance targets.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

To design an operational I/O power domain with these cells, an additional library is required – 1.8V Support: Power. That library contains an input-only buffer, isolated analog I/O, and a full complement of power cells along with corner and spacer cells to assemble a functional pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

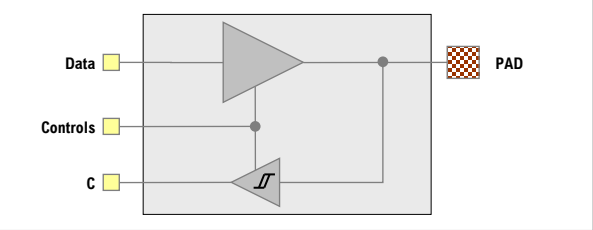
Cell Size & Form Factor

- Staggered (pad-limited) – 17.04µm x 191.28µm
- Flip chip implementation with CUP structure built in

Recommended operating conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.675	0.75	0.825	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
		1.35	1.5	1.65	V
		1.08	1.2	1.32	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

SRP_BI_SDS_18V_STB



Bidirectional GPIO Driver Features

- Multi-voltage (1.2V, 1.5V, 1.8V)
- LVCMOS / LVTTL input with selectable hysteresis
- Programmable drive strength (rated 2mA to 12mA)
- Selectable output slew rate
- Optimized for EMC with SSO factor of 8
- Open-drain output mode
- Programmable input options (hi-Z/pull-up/pull-down/repeater)
- Power sequencing independent design with Power-On Control

In full-drive mode, this driver can operate to frequencies in excess of 100MHz with 15pF external load and 125 MHz with 10pF load. Actual frequency limits are load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

Characterization Corners

Model [1]	LPE Type	VDD=0.75V	DVDD [2]	Temp
FF	Cbest_CCbest	+10%	+10%	-40°C
FF	Cbest_CCbest	+10%	+10%	0°C
FF	Cbest_CCbest	+10%	+10%	125°C
FFG	Ctypical	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SS	Cworst_CCworst	-10%	-10%	-40°C
SS	Cworst_CCworst	-10%	-10%	0°C

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.
[2] DVDD = 1.8V, 1.5V & 1.2V

Published by:

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