TSMC 06/07: LPDDR2/3/4_DDR3/4

Libraries

Name	Process	Form Factor
RGO_TSMC06_18V15_6FF_25F_DDR4_7WC	6FF	Staggered Flip Chip
RGO_TSMC07_18V15_7FF_25C_DDR4_7WC	7FF	Staggered Flip Chip

Summary

The LPDDR2/3/4_DDR3/4 library provides 7-way combo DDR driver/receiver cells with embedded power cells, the driver impedance calibration cell, and the DDR voltage reference cell providing both single-ended and differential signaling for LPDDR2, LPDDR3, LPDDR4, DDR3, DDR3L, DDR3U, and DDR4 applications. Also included is a full complement of power, corner and spacer cells to assemble a functional pad ring by abutment. An included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

This library is offered at both 6nm and 7nm. It is available in a staggered flip chip implementation.

Full DDR4 capability
- Data rates – 1600 MT/s, 1866 MT/s, 2133 MT/s, 2400 MT/s

Full DDR3 / DDR3L / DDR3U capability
- Data rates – 800 MT/s, 1066 MT/s, 1333 MT/s, 1600 MT/s, 1866 MT/s, 2133 MT/s

Full LPDDR4 capability
- Data rates – 1066 MT/sec, 2400 MT/sec, 3200 MT/sec, 4266 MT/sec

Full LPDDR3 capability
- Data rates – 1333 MT/sec, 1600 MT/sec

Full LPDDR2 capability
- Data rates – 466 MT/sec, 1066 MT/sec

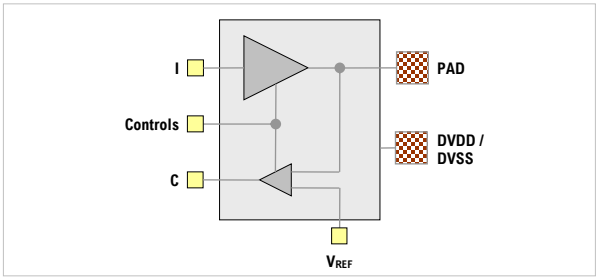
ESD Protection:
- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

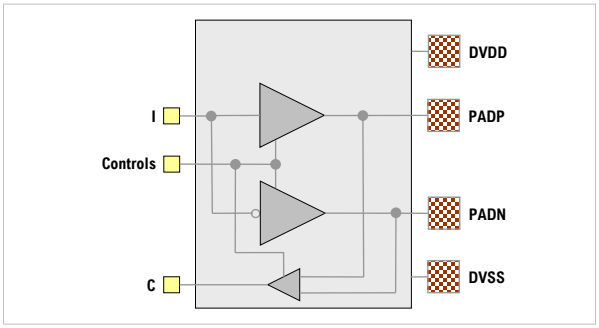
Cell Size & Form Factor

- Staggered (pad-limited) – 50.4µm x 398.976µm
- Flip chip implementation with CUP structure built in

SLP_BI_SDS_1215V_D _x: Single-Ended Driver



SLP_CL_SDS_1215V_D_PWR : Differential Driver



DDR Driver Features

- User programmable drive strength
  - DDR3 – Z_{OUT} = 34 / 40 Ω
  - DDR3L – Z_{OUT} = 34 / 40 Ω
  - DDR3U – ZOUT = 34 / 40 / 48 / 60 / 80 Ω
  - DDR4 – Z_{OUT} = 34 / 48 Ω
  - LPDDR2 – Z_{OUT} = 34 / 40 / 48 / 60 / 80 Ω
  - LPDDR3 – Z_{OUT} = 34 / 40 / 48Ω
  - LPDDR4 – Z_{OUT} = 40 / 48 / 60 / 80 / 120 / 240 Ω
- User programmable on-die termination
  - DDR3 – 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
  - DDR3L – 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
  - DDR3U – 120 / 60 / 40 / 30 / 24 / 20 / 17 Ω
  - DDR4 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
  - LPDDR3 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
  - LPDDR4 – 240 / 120 / 80 / 60 / 48 / 40 / 34 Ω
- Operating frequency up to 2133 MHz (4266 MT/sec) data rate)
- Power sequencing independent design with Power-On Control

Recommended Operating Conditions

Parameter	Description		Min	Nom	Max	Units
V_{VDD}	Core supply voltage		0.675	0.75	0.825	V
V_{DVDD}	I/O supply voltage	DDR4	1.14	1.2	1.26	V
		DDR3	1.425	1.5	1.575	V
		DDR3L	1.283	1.35	1.45	V
		DDR3U	1.19	1.25	1.31	V
		LPDDR2	1.14	1.2	1.3	V
		LPDDR3	1.14	1.2	1.3	V
		LPDDR4	1.06	1.1	1.17	V
T_J	Junction temperature		-40	25	+125	°C
V_{PAD}	Voltage at PAD		V_{DVSS}		V_{DVDD}	V

Characterization Corners

Model	LPE Type	VDD	DVDD	Temp
FF	Cbest_CCbest	+10%	See table below for DVDD voltage ranges.	-40°C
FF	Cbest_CCbest	+10%		0°C
FF	Cbest_CCbest	+10%		125°C
FFG	Ctypical	+10%		125°C
TT	Ctypical	nominal		25°C
TT	Ctypical	nominal		85°C
SS	Cworst_CCworst	-10%		-40°C
SS	Cworst_CCworst	-10%		0°C
SS	Cworst_CCworst	-10%		125°C

[1] Listed models are for 7FF. 6FF models are FFGNP / TT / SSGNP.

Characterization DVDD Voltage Ranges

Nominal DVDD		FF	TT	SS	Units
1.2	DDR4	1.26	1.2	1.14	V
1.5	DDR3	1.575	1.5	1.425	V
1.35	DDR3L	1.45	1.35	1.283	V
1.25	DDR3U	1.31	1.25	1.19	V
1.2	LPDDR2	1.3	1.2	1.14	V
1.2	LPDDR3	1.3	1.2	1.14	V
1.1	LPDDR4	1.17	1.1	1.06	V

Cell summary

Name	Description
SLP_BI_SDS_1215V_D_DVDD/DVSS/PDO	Single-ended driver / receiver with power
SLP_CL_SDS_1215V_D_PWR	Differential clock driver / receiver with DVDD / DVSS
SLP_SP_CAL_SDS_1215V	DDR calibration cell
SLP_SP_CSH_0915V	Calibration code bus driver
SLP_RE_000_1215V	DDR voltage reference
PVP_VD_RCD_0915V	Core power (VDD)
PVP_VS_RCD_0915V	Core ground (VSS)
SVP_SP_000_1215V	0.1 µm spacer
SVP_SP_001_1215V	1 µm spacer
SVP_SP_005_1215V	5 µm spacer
SVP_SP_020_1215V	20 µm spacer
SVP_CO_001_1215V	Corner cell
SPP_RS_005_1215V	Rail splitter
SPP_AD_SSTL_1215V	DDR to staggered 1.8V GPIO adapter
SPP_SP_CAP_1215V	DVDD/DVSS decoupling cap

Published by:

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