TSMC 05: 1.8V Support: Power

Libraries

Name	Process	Form Factor
RGO_TSMC05_15V18_N5_45F_SPT	N5	Inline

Summary

This 1.8V Support: Power library provides a full complement of cells to support the assembly of a functional pad ring by abutment. It is supplied as a standard addition to the GPIO libraries and other I/O library offerings from Aragio Solutions that use a compatible pad ring bus structure.

The library is available in an inline flip chip implementation.

The included rail splitter allows multiple power domains to be isolated in the same pad ring while maintaining continuous VDD/VSS for robust ESD protection.

ESD Protection:

- JEDEC compliant
  - 2kV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)

Latch-up Immunity:

- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

- Inline (core-limited) – 66.5µm x 100.1µm
- Flip chip implementation with CUP structure built in

Cell List

Name	Description
I/O Power / Ground Pads	
PWC_VD_RDO_1218V	I/O power (DVDD)
PWC_VS_RDO_1218V	I/O ground (DVSS)
Core Power / Ground Pads	
PWC_VD_RCD_1018V	Core power (VDD)
PWC_VS_RCD_1018V	Core ground (VSS)
Analog Pads *	
ANC_BI_DWR_1218V	1.8V Analog Input cell
Analog Power / Ground Pads	
PWC_VD_ANA_1018V	Analog power (AVDD) 1.0V
PWC_VS_ANA_1018V	Analog ground (AVSS)
PWC_VD_ANA_1218V	Analog power (ADVDD) 1.8V
PWC_VS_ANA_1218V	Analog ground (ADVSS)
Support Pads	
SPC_SP_P028_1218V	0.028µm spacer
SPC_SP_P038_1218V	0.038µm spacer
SPC_SP_P084_1218V	0.084µm spacer
SPC_SP_001_1218V	1µm spacer
SPC_SP_002_1218V	2µm spacer
SPC_SP_005_1218V	5µm spacer
SPC_SP_010_1218V	10µm spacer
SPC_RS_005_1218V	Rail splitter
SPC_RE_SVR_1218V	VREF / HVPS generation
SPC_SP_POC_1218V	POC generation

Recommended Operating Conditions

	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.675	0.75	0.825	V
		0.765	0.85	0.935	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
		1.35	1.5	1.65	V
		1.08	1.2	1.32	V
T_J	Junction temperature	-40	25	125	°C
V_{PAD}	Voltage at PAD	V_{DVSS} -0.3	-	V_{DVDD} +0.3	V

Characterization Corners

Model	LPE Type	VDD [1]	DVDD [2]	Temp
FFGNP	Cbest_CCbest	+10%	+10%	-40°C
FFGNP	Cbest_CCbest	+10%	+10%	0°C
FFGNP	Cbest_CCbest	+10%	+10%	125°C
TT	Ctypical	nominal	nominal	25°C
TT	Ctypical	nominal	nominal	85°C
SSGNP	Cworst_CCworst	-10%	-10%	-40°C
SSGNP	Cworst_CCworst	-10%	-10%	0°C
SSGNP	Cworst_CCworst	-10%	-10%	125°C

[1] VDD = 0.75V & 0.85V
[2] DVDD = 1.2V, 1.5V & 1.8V

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